OPTIMAL DESIGN AND PERFORMANCE EVALUATION OF DEVICES BEYOND BULK CMOS

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BY

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Certificate

Certified that this work entitled **"OPTIMAL DESIGN AND PERFORMANCE EVALUATION OF DEVICES BEYOND BULK CMOS"** which is being submitted by **Mr. MOHD AJMAL KAFEEL**, in partial fulfillment of the requirements for the award of the degree of **DOCTOR OF PHILOSOPHY IN ELECTRONICS ENGINEERING** from Aligarh Muslim University, Aligarh, India. This is a record of candidate's own work under our supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

Prof. M. Shah Alam **Prof. Mohd. Hasan**

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I would like to express my deep gratitude and appreciation to my supervisor, Prof. Mohd. Hasan. His vision and approach towards research, directed towards "doing what is important and will provide help to the scientific community," helped me understand how to acquire and use my problem solving skills and attitude. His guidance, through strict professionalism as well as care towards his students, is really admirable, and constitutes true mentoring lessons, beyond the scientific aspect.

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I whole-heartedly express my feeling of appreciation to Mrs Iffat Ara Bano and Dr. Salma Shaheen for encouraging me and providing me every possible help to avail leave in order to complete this research work.

All of this was made possible by the love and encouragement of my family members. Last but not the least, I would like to acknowledge the love and continual encouragement of my mother and father, and the strong support of my beloved wife Shazia and my mother in law who helped me to carry out my research work unperturbed. Finally, I am extremely thankful for the immense love and understanding from the part of my heart, my son Sarim and daughter Sophia.

(MOHD. AJMAL KAFEEL)

ABSTRACT

In current bulk CMOS technology, semiconductor devices are continuously scaled down as per the Moore's law to achieve higher speed and packing density. This continuous scaling of MOSFET below 45nm technology node gives rise to short channel effects like Drain induced barrier lowering (DIBL), threshold voltage (V_t) roll off, random dopant fluctuations, mobility degradation etc. along with increased power consumption. There is also pressing need to design low power circuits due to rapid growth of portable devices for extending their battery life. This demands the supply voltage (V_{DD}) to be scaled along with device dimensions. As device dimensions especially the oxide thickness (T_{OX}) is reduced along with the supply voltage, in order to maintain better electrostatic control over channel, several gate leakages due to Fowler-Nordheim and direct tunnelling, hot carrier injection occur. Therefore, VLSI circuits and systems need serious attention while designing in sub-45 nm technology node. Although multiple gate transistors and strained silicon devices overcome some of the bulk CMOS problems, it is sensible to look for revolutionary new materials and devices to replace silicon. It is obvious that future technology materials should exhibit higher mobility, better channel electrostatics, scalability and robustness against process variations.

This thesis starts with the optimization and characterization of CMOS device parameters like substrate doping, channel length, oxide thickness and halo doping concentrations of MOSFET at 45nm technology node using Synopsys Sentaurus TCAD tools under subthreshold condition for the better performance of the circuit.

Tunneling Field Effect Transistor (TFET) is considered as one of the most promising device to provide scaling benefits with significant reduction in short channel effects. It is an attractive candidate for low voltage CMOS devices due to the ability to achieve steep subthreshold swing, below the 60 mV/decade limit of the MOSFET. In this thesis, both the n and p-type TFETs using germanium as source material are designed and simulated using Sentaurus TCAD for an effective channel length of 25nm. The performance of these TFET devices are analysed by designing the Current conveyor (CCII), which is considered to be the main building block of the analog world. The performance parameters of TFET based CCII are much better as compared

to its CMOS counterpart thereby, making it an extremely attractive option for ultra-low voltage biomedical applications.

Recently, carbon nanotube based technology is also a promising choice to replace the CMOS technology for designing nanoscale circuits and systems and comparing its performance with existing bulk CMOS for its rapid commercialization. Therefore, this work also investigates and optimizes the performance of these upcoming devices by proposing a single ended 6-T SRAM cell that saves dynamic as well as static power and maintains higher read stability at the cost of acceptable read/write delay. It proves its robustness by exhibiting narrower spread in various design metrics. Finally, a four quadrant analog multiplier based on memristors, which is considered to be another emerging device that has caught the attention of researchers of late, and optimized CNFETs is proposed which is capable of high bandwidth and low power operation as compared with other CMOS based multipliers.

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Introduction

Chapter 1

INTRODUCTION

This introductory chapter starts with the motivation of this research work in section 1.1. It then briefly explains the contributions made during the research in section 1.2. Finally, section 1.3 outlines the structure of this thesis.

1.1 Motivation

The scalability of semiconductor manufacturing has shown the continued improvement in the performance of metal-oxide-semiconductor field effect transistor (MOSFET). A schematic diagram of MOSFET is presented in Figure 1.1. The gate electrode alters the channel resistance by capacitive coupling of the semiconductor region immediately below the gate with a bias applied between the source and the drain regions. This gate behavior controls a source side energy barrier, modulating the current flowing from the source to the drain as shown in Figure 1.2.

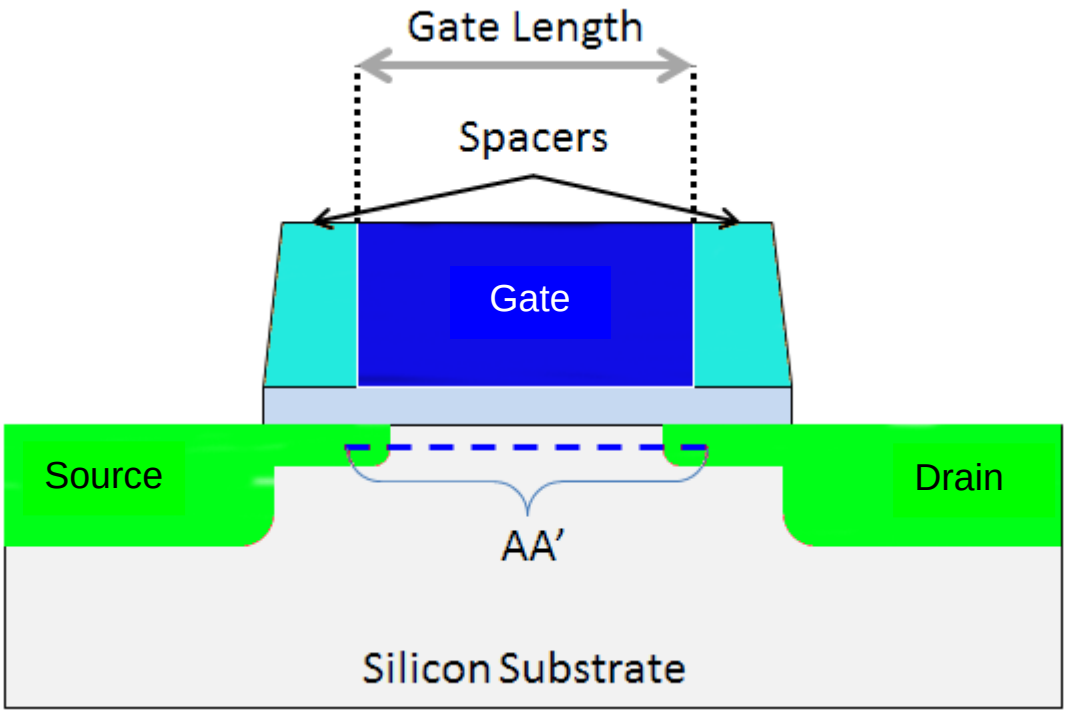

Figure 1.1: Schematic diagram of a MOSFET.

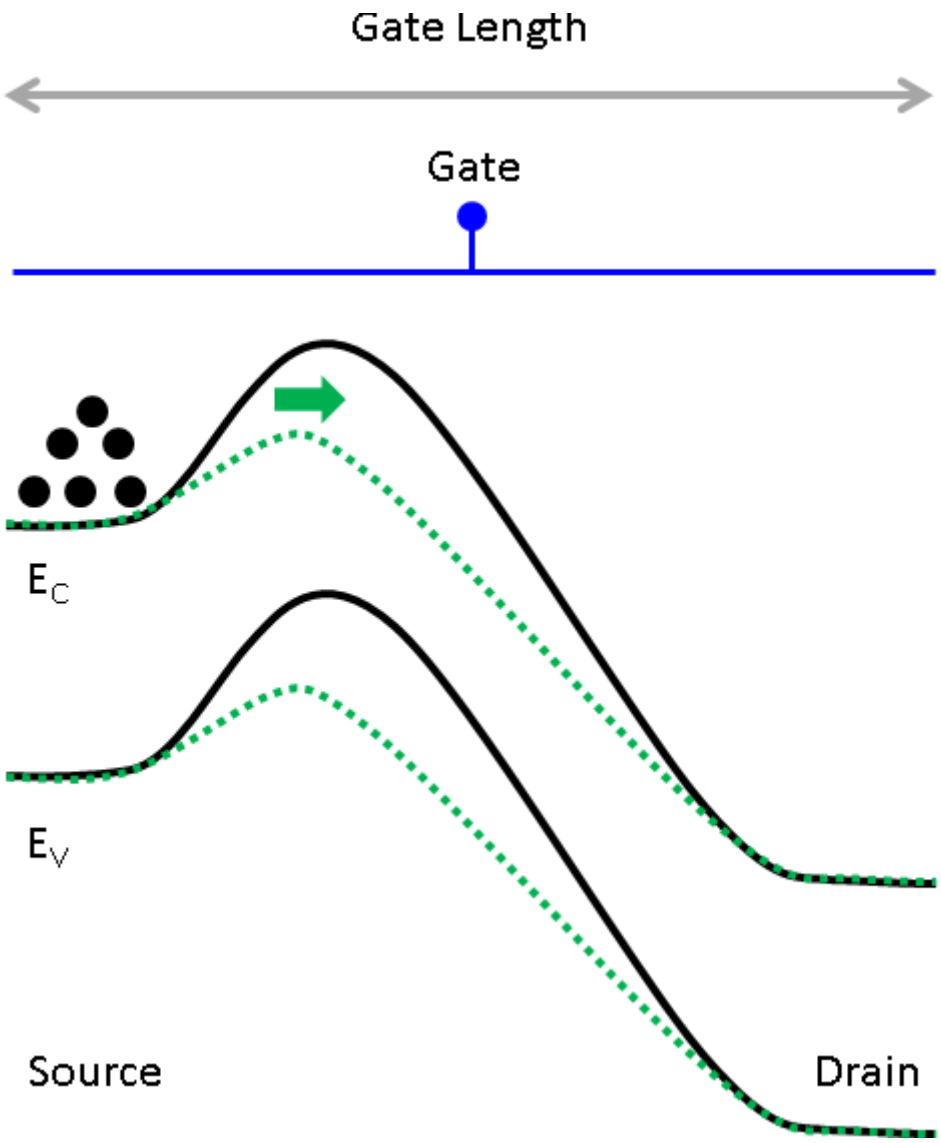

Figure 1.2: A Band diagram of a MOSFET corresponding to AA' cut line in Figure 1.1.

For over 40 years, the electronics industry has followed Moore's law [1] to improve the device performance and density. As shown in Figure 1.3., the number of transistors per chip doubles approximately every two years. Thus, scaling involved decreasing the channel length (L_g) and gate oxide thickness (T_{OX}) so as to increase the current drive of the transistor. However, if only these two parameters are scaled many problems are encountered, e.g., increased electric field. In 1974, Dennard[3] developed guidelines for scaling which maintains an electric field in the device constant. This constant field scaling has not been observed in reality and ended in mid-2000 and the industry moved into power constrained scaling.

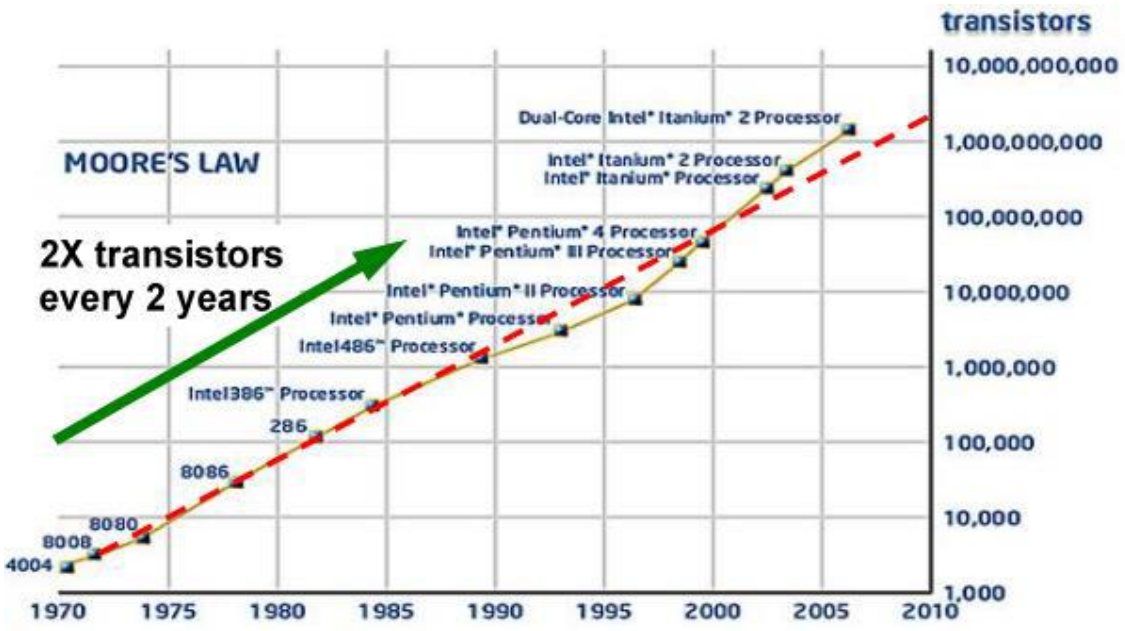

Figure 1.3: Number of Transistors on Intel Processor versus year of release of that processor [2].

In this regime, supply voltage (V_{DD}) of the transistor has not scaled with other device parameters and dimensions. This is due to the fact that the threshold voltage (V_t) must be scaled along with supply voltage in order to maintain sufficient I_{ON}/I_{OFF} ratio. Scaling of V_t however, results in exponential increase in the off state leakage current. This increase in the off current is due to constant subthreshold swing (SS) of the MOS transistor, which is defined by $SS = (d\log I_D/dV_{GS})^{-1}$ as the measure of the inverse slope of the I_D-V_{GS} curve below threshold. Moreover, there is a theoretical limit for MOSFET of $\log(10)kT/q$ = 60 mV/decade, where k is the Boltzmann's constant, T is temperature in Kelvin, and q is the electron charge. As a result of constant voltage scaling, power density increases with circuit speed or transistor density. This is of great concern particularly in today's world of mobile electronics where battery life and cooling constraints set limits on allowable power dissipation.

In order to continue scaling of CMOS devices, there is a need to explore new devices that use other mode of carrier transport at a supply voltage of less than 0.5V together with lower subthreshold swing (<60mV/decade) that maintains high on current with reduced off state current that compete directly with their CMOS counterparts in terms of power, area and speed [4]. The other modes of carrier transport and device architectures with steeper SS include impact ionization [5-6], inter-band tunnelling transistor [7], ferroelectric FET [8].

This thesis explores options for continued scaling by investigating two promising transistors namely Tunneling Field-Effect Transistor (TFET) and Carbon Nano tube Field-Effect Transistor (CNFET). The TFETs, also known as steep slope transistors, have SS less than 60mV/decade. These devices can meet OFF current requirements at lower supply voltages, thereby, leading to lower OFF state leakage and power dissipation than CMOS at the same supply voltage.

CNFETs, on the other hand, offer lower leakage, lower variability and better electrostatic control over the channel region. It exhibits ballistic transport of carriers that results in high on current at lower supply voltages.

1.2 Contributions

This thesis is aimed at analyzing and exploring TFET and CNFET devices that can work at lower supply voltages to reduce leakage and provide higher I_{ON}/I_{OFF} ratio.

The following are the key contributions made in this thesis while designing and optimizing TFET and CNFET circuits for ULP applications.

- This thesis proposes new device process parameters using Synopsys TCAD to improve the subthreshold slope and I_{ON}/I_{OFF} ratio to enhance the speed of CMOS subthreshold circuits as device designed for super-threshold circuits is not optimum under subthreshold conditions.

- Furthermore, this thesis presents the design and optimization of ultra-low power CMOS based second generation current conveyor (CCII) in the subthreshold region at 32nm technology node. Optimal sizing of transistors for different designs has been done at low supply voltages.

- The design and performance evaluation of CMOS and TFET based Second Generation Current conveyor (CCII) at a supply voltage of ±0.3V and bias current of 1nA at 32nm technology node is presented. It exhibits considerable improvement in most of the performance parameters of CCII using TFET.

- This work proposes a CNFET based single ended 6T SRAM cell that saves dynamic as well as static power and maintains higher read stability at the cost of acceptable read/write delay. It proves its robustness by exhibiting narrower spread in various design metrics.

- It also introduces the concept of memristors and proposed a reconfigurable memristor and CNFET based four quadrant analog multiplier capable of high bandwidth and low power operation.

1.3 Thesis organization

The core chapters of this thesis, from Chapter 3 to Chapter 7, are a collection of manuscripts published in refereed journals. This thesis specially targets the design and optimization of the beyond CMOS devices like TFETs and CNFETs particularly for low power applications. The structure of this thesis is as follows:

- Chapter 2 starts with a discussion on short channel effects and subthreshold swing. It then describes the operating principle of TFET in detail and reviews selected prior research work.

- Chapter 3 primarily investigates the effect of different process parameters on the performance of NMOS device design metrics using TCAD under subthreshold conditions. It then optimizes the NMOS device for better value of subthreshold slope and improved I_{ON}/I_{OFF} ratio.

- Chapter 4 presents the design and optimization of ultra-low power second generation current conveyor (CCII), operating in the subthreshold region of CMOS. Optimal sizing of transistors for different designs has been done at low supply voltages.

- Chapter 5 investigates design and performance analysis of Tunnel Field Effect Transistor (TFET) Based Current Conveyor for Ultra Low Power Biomedical Applications. The performance parameters of CCII have been investigated in terms of current gain (α), voltage gain (β), current and voltage bandwidths, resistances and their respective bandwidths at various ports of CCII.

- Chapter 6 explores performance evaluation of CNFET based single ended 6T SRAM cell. It is observed during the investigation that CNFET based 6T SRAM cell proves its robustness by exhibiting narrower spread in various design metrics as compared with CMOS based SRAM cell. This is due to the cylindrical geometry of a CNFET. A variation in the gate oxide thickness that

strongly affects the drive current and capacitance of CMOS has negligible impact on CNFET's operation.

- Chapter 7 presents a reconfigurable, low power four quadrant memristor and carbon nanotube field effect Transistor (CNFET) based analog multiplier. The proposed multiplier is operated at low supply voltage providing extremely large bandwidth and consuming very little power.

- Chapter 8 presents conclusions and a summary of the thesis and suggests topics for future research.

The next chapter reviews the discussion on subthreshold swing and various shortcoming of MOSFET. It then presents an operating principle of TFET and some literature review on TFETs.

CHAPTER 2

Background and Previous Work

Chapter 2

BACKGROUND AND PREVIOUS WORK

2.1 Introduction

Scaling of CMOS technology is done in order to meet the performance, cost, and power requirements of forthcoming high throughput applications [9]. This has been made possible by steady progress in planar processing technology to manufacture transistors with even smaller dimensions, resulting in an exponential growth in number of transistors on a single chip and, hence, functionality of ICs as per Moore's law [10]. The electronic industry has remarkably kept pace with this exponential growth for the last four to five decades. This exponential growth of transistors count cannot continue for ever as pointed out by Moore's himself in 2003 [11]. Therefore, many experts are now claiming that CMOS scaling has reached its limits. There are three factors that limit CMOS scaling:

1) Smaller or minimum dimensions that can be fabricated on a chip

2) Diminishing returns in switching performance of scaled CMOS device

3) Static or off state leakage power.

The primary limitations for CMOS scaling have been associated with the process of lithography i.e. how small a transistor can be fabricated on a chip. Advancement in the technology has demonstrated the use of 193nm wavelength to pattern 45nm transistors [12]. Further advancement has opened up the possibility of using Extreme ultraviolet lithography (also known as EUV or EUVL) as the next generation lithography using an extreme ultraviolet (EUV) wavelength. This is targeted to be used for future technologies below 15nm [13-14], resulting in the exponential rise of the cost of lithographic equipment that will limit the profitability of increased scaling.

Due to CMOS scaling, transistor dimensions are approaching the limits of atom or molecule and clearly, it cannot be less than that limit. This aggressive scaling severely affects the electron and hole mobilities which means that the performance gains from each successive generation is less than the gain from the last generation.

The final and the most significant factor that limits MOS scaling is the static or OFF state power consumption. The sources that contribute to OFF state leakage are: junction leakage, gate induced drain leakage, subthreshold current and gate tunnel currents. They become more and more pronounced as the dimensions are scaled. It was shown in [12] that the leakage currents grow exponentially as gate length is reduced.

As depicted in Figure 2.1, although technology scaling reduces the dynamic power dissipation, there is a marked increase in the subthreshold leakage power which may exceed the active power for future technology nodes around 10nm node [15]. Technology scaling trends, as dictated by Moore's law, has pushed power consumption to the forefront for circuits having limited power budget. Negligible amount of dynamic power dissipation takes place when CMOS transistor is not switching at higher technology nodes. Nevertheless, static power dissipation increases appreciably which is primarily due to the flow of leakage current under subthreshold condition. Therefore, some special class of applications, which are bound by ULP budget, can be accomplished by operating circuits in the subthreshold region. This chapter briefly reviews the sources of power consumption at the nanometer scale with respect to the subthreshold region. It then also focuses on the basics of upcoming devices like TFETs and CNFETs to replace CMOS followed by the review of selected prior art.

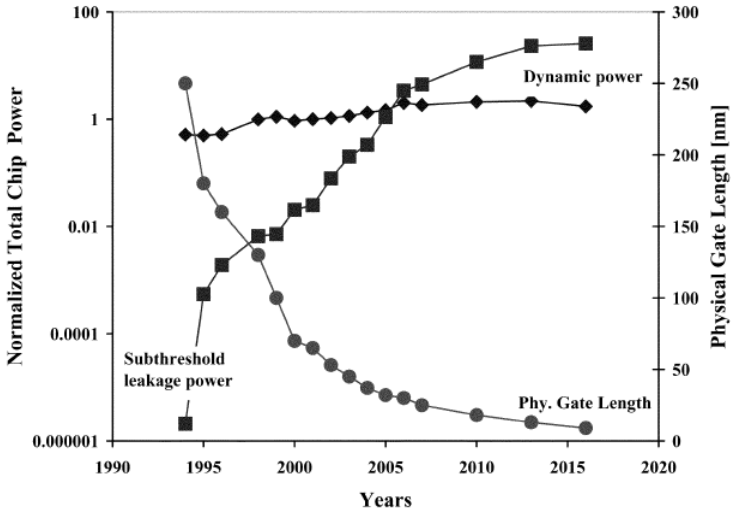

Figure 2.1: Normalized dynamic and static power dissipation for (*W/Lg*=3) device. Data is based on the ITRS [9].

2.2 Sources of Power Consumption in CMOS

Sources of power consumption can be divided into two major types:

1) Dynamic power consumption

2) Static power consumption

The difference between the two is that while the dynamic power is proportional to the activity in the circuit and the switching frequency, whereas the static power is independent of both. The power consumed in any CMOS logic must be reduced for the following two reasons. First it is important to reduce the dissipation of heat to allow a large density of the components to be fabricated on an IC chip. Second one is to conserve energy of the battery operated systems in order to enhance the battery life time. This section briefly reviews dynamic and static power in detail along with different leakage currents.

2.2.1 Dynamic Power Consumption

Dynamic power consumption occurs when internal node (s) of a circuit switches due to changes in the input vector (s). It is caused by two different categories of current: load capacitance (C_L) charging/discharging current and short circuit current. Therefore, it consists of two components namely switching power and short circuit power [16].

1. Switching power

Switching power can be described best with the help of CMOS inverter as shown in Figure 2.2. Assuming the initial input vector to be '1', then the voltage across the load capacitance is '0' as it is fully discharged by the pull-down NMOS. If from this steady state condition, the input vector is changed to '0', then the NMOS stops conducting and PMOS starts conducting, thereby, charging C_L gradually to V_{DD}. The switching power consumption due to capacitive current is given by [16]:

$$P_{dyn} = \alpha f C_L V_{DD}^2 \tag{2.1}$$

where 'f' is the clock frequency, and 'α' is the activity factor. It is to be noted that, C_L is the parasitic capacitance of the output node of the inverter. C_L is composed of three components: drain diffusion capacitance of both the MOSFETs, capacitance of the

connecting wires, and the input capacitance of the fan out gates. The energy drawn from V_{DD} is totally lost in the complete charging and discharging cycles. Equation (2.1) shows that the power consumption is a quadratic function of V_{DD} and hence, the most significant reduction in power dissipation is achieved by V_{DD} reduction technique.

2. Short-Circuit Power

During the transition of signal, both pull up and pull down devices conduct simultaneously for a short duration of time which temporarily results in short-circuit path from supply to ground within gate. The simplest static CMOS inverter is shown in Figure 2.2. When NMOS transistor turns ON due to the rising input then the PMOS transistor also continues to conduct current until the input voltage becomes greater than $V_{DD}- |V_{tp}|$. Hence, a direct current flow from supply to ground, which is called as short-circuit current [17]. The total charge that flows in this period can be found by calculating the area of the triangle [18] as shown in Figure 2.2 . Let 't_r' denotes the time for the input voltage to rise from V_{tn} to $V_{DD}- |V_{tp}|$. V_{tn} and V_{tp} is the threshold voltage of NMOS and PMOS transistors respectively. Assuming symmetric rise and fall transitions for both input and output of the logic gate, the total short-circuit power consumption due to short circuit current as shown in Figure 2.3 for a single logic gate is defined as [16]:

$$P_{SC} = \alpha t_r V_{DD} I_{peak} f \tag{2.2}$$

Where 'α' is the switching activity factor, I_{peak} is the peak current per transistor width.

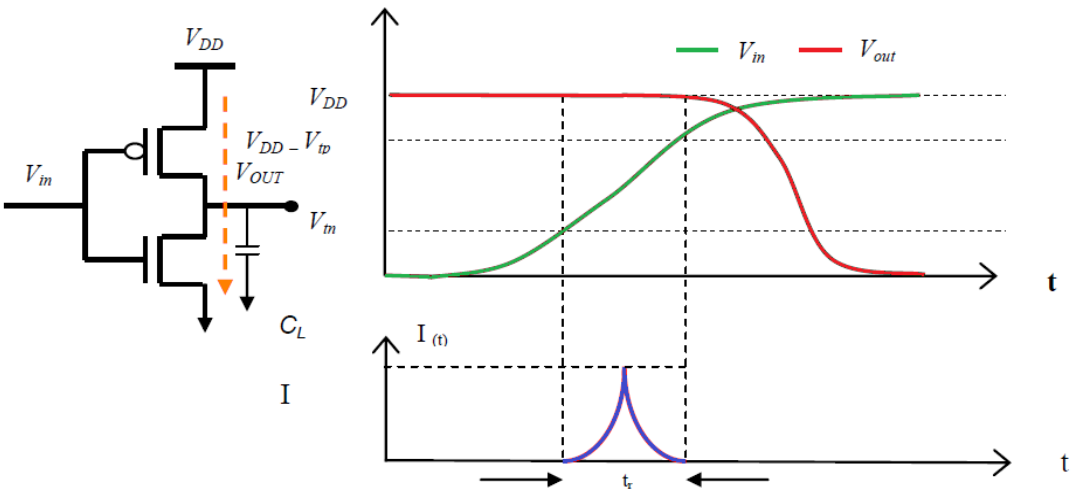

Figure 2.2: Schematic of inverter with voltage and current waveforms.

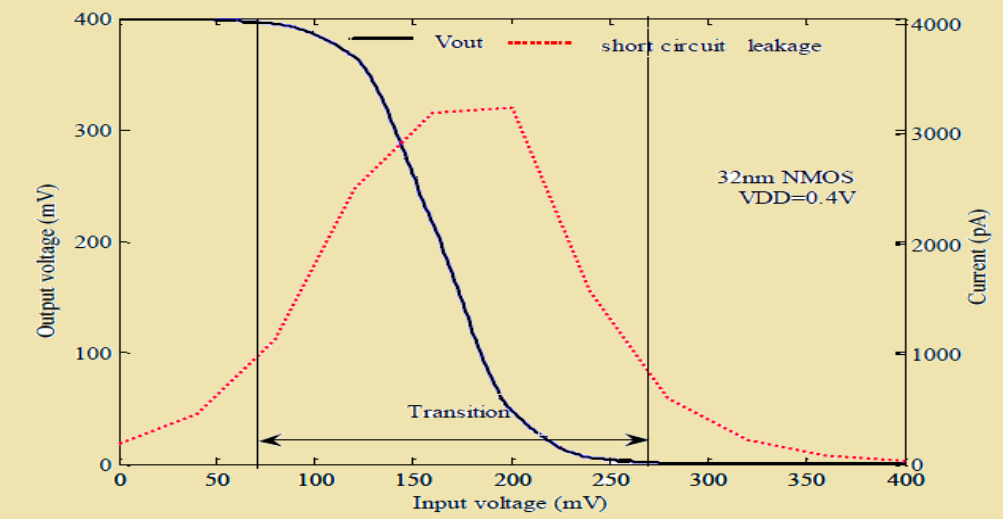

Figure 2.3: Short circuit leakage current of inverter at 32 nm technology node.

2.2.2 Static Power Consumption

The static power ($P_{static} = I_{static} \times V_{DD}$) is defined as the power consumption due to constant current from V_{DD} to ground in the absence of any switching activity [16]. Ideally, this static power consumption in a CMOS circuit is zero, as devices in PUN (pull-up network) and PDN (pull-down network) are never switched ON simultaneously in steady state conditions. This type of dissipation is negligible for long channel transistors with high V_{th}. Unfortunately, present and future technologies will suffer from high static power, which could even exceed the dynamic contribution in active mode [19]. Shrinking device dimensions causes different sources of leakage current [9]. Different leakage current components contributing to leakage power dissipation through a short channel NMOS transistor are shown in Figure 2.4 [20] and are briefly described here:

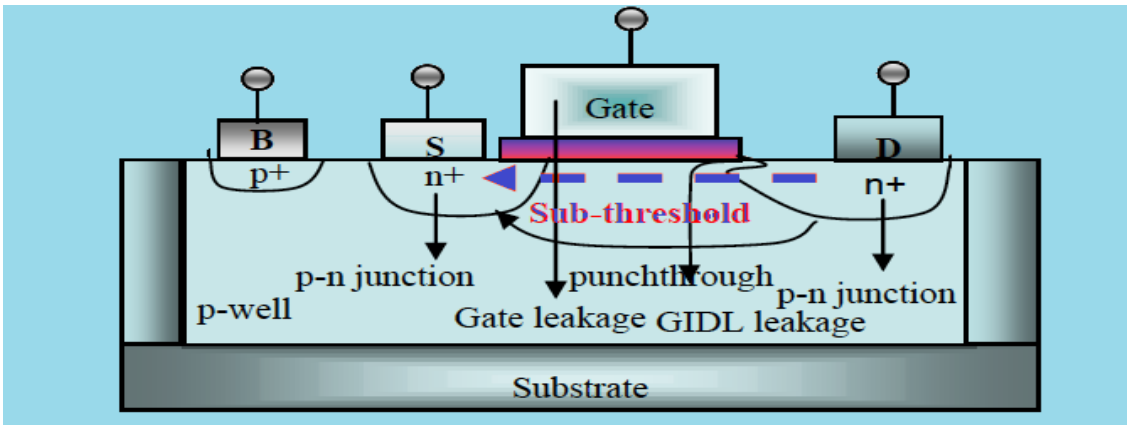

Figure 2.4: Leakage current mechanisms in an NMOS transistor.

1. Reverse bias pn junction current and band to band tunneling leakage current

Normally in a MOS transistor as shown in Figure 2.4, drain/source to well junction is reverse biased which causes pn junction leakage current. This current is originated because of the minority carrier drift/diffusion near the edge of the depletion region and due to electron-hole pair generation in the depletion region of the reverse biased junction [21-22]. The magnitude of the diode's leakage current depends on the area of the drain diffusion and the leakage current density, which in turns is determined by the doping concentration. If both n and p regions are heavily doped, band-to-band tunneling (BTBT) dominates the pn-junction leakage [23].BTBT leakage current flows under high electric field ($>10^6$ V/cm) across the reverse biased pn junction.

Process technologies are generally well designed to keep this pn junction leakage small relative to the subthreshold current. Since the pn-junction leakage scales with V_{DD} and temperature in a similar fashion as subthreshold current, pn-junction leakage is negligible across the full range of V_{DD} under subthreshold conditions [24].

2. Subthreshold leakage current

The origin of subthreshold leakage current is due to the process of diffusion of minority carriers in a non-conducting transistor when $V_{GS} < V_{th}$. Under this condition, the MOS transistor is operated in weak inversion mode [25-26]. Difference of potential between the drain and source creates a flow of minority carriers on the surface of the channel. The subthreshold current is exponentially dependent on V_{th}. This is the reason why the low V_{th} characterizing technologies lead to large subthreshold current.

3. Gate leakage current

Due to scaling, oxide thickness (T_{OX}) is progressively getting thinner. As T_{OX} scales below 3 nm, gate to channel leakage current starts to appear even at low gate voltage. This results in direct tunneling of electrons through the gate oxide as depicted in Figure 2.4. The gate leakage is present in both the OFF state and the ON state of a MOS transistor, which makes it more difficult to control than subthreshold leakage [178-180]. Gate leakage is the sum of two components namely the gate to channel and the gate to source/drain extension overlap current in the ON state. However, in the

OFF state, it is due to the edge direct-tunneling current (EDT). This leakage current increases exponentially with the T_{OX} reduction due to the increasing tunneling probability that depends strongly on the voltage across the oxide. The gate leakage is expressed by the following equation [28]

$$I_{gate} = W_{eff} L_{eff} A(\frac{V_{ox}}{T_{ox}})^2 \exp\left[\frac{-B(1-(1-V_{ox}/\phi_{ox})^{3/2}}{V_{ox}/\phi_{ox}}\right] \quad 2.3$$

Where, $$A = \frac{q^3}{16\pi h\phi_{ox}}, B = \frac{4\sqrt{2m}\phi_{ox}^{3/2}}{3hq}$$

'V_{ox}' is the potential drop across the thin oxide layer, 'ϕ_{ox}' is the barrier height for the tunneling particles, 'T_{OX}' is the oxide thickness, and 'A and B' are physical parameters.

Gate tunneling current has a very strong dependence on the voltage across the gate. Hence, it decreases much more quickly with V_{GS} and V_{DD} as compared to the subthreshold current.

4. Gate-Induced Drain Leakage current

A high electric field exists in the overlapping zone between gate and drain which leads to the generation of current from the edge of drain and terminates at the body of the transistor. Consider an NMOS transistor, when a low gate potential is applied (V_G ≈0V), holes accumulate at the surface and create a region which is more heavily p doped than the substrate. If this happens while the drain is connected to a high potential (V_{DD}), the depletion layer near the drain becomes narrower. As a result of this, minority carriers are emitted in the drain region underneath the gate and pushed to the substrate due to the vertical electric field as shown in Figure 2.5. Thinner T_{OX} and higher potential between gate and drain enhance the electric field thereby increasing Gate-Induced Drain Leakage (GIDL) [24].

The lower values of V_{DS} for subthreshold operation decreases the electric field across the drain, hence, GIDL current component becomes negligible.

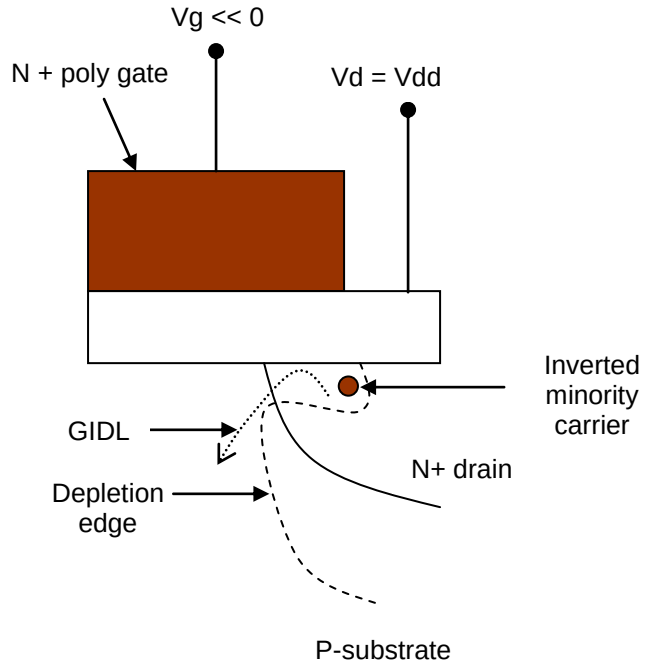

Figure 2.5: Gate-induced drain leakage mechanism in a MOSFET.

5. Drain induced barrier lowering(DIBL) and Punchthrough Leakage current

Due to the proximity of source and drain in short channel devices, the depletion regions at the drain-substrate and source-substrate junctions extend into the channel. As the channel length is reduced for a fixed doping level, the separation between the depletion region boundaries decreases. An increase in the reverse bias across junctions (with increase in V_{DS}) also pushes the junctions nearer to each other, resulting in an increase in leakage current. This phenomenon is sometimes refers to as DIBL. This may lead to large flow of current called as punchthrough leakage current.

Though these leakage components are quite significant for strong inversion operation, they tend to become negligible under subthreshold conditions where subthreshold leakage is more pronounced [24]. However, gate leakage dominates subthreshold leakage current at very low temperature as it decreases exponentially with temperature**.**

In order to try to reduce the power dissipation of CMOS, circuit engineers change their circuits, and device engineers change their devices. The bulk of this thesis is about devices, so it would be appropriate to look into new transistor operating principles which can reduce power dissipation in integrated circuits. As far as CMOS

is concerned, one way to reduce power dissipation is to operate the optimized device in subthreshold region. Based on this optimization and characterization of CMOS, particularly for subthreshold region, we have published a paper which will be covered in chapter 3. The next section briefly discusses about two upcoming devices namely TFETs and CNFETs.

2.3 Introduction to the Tunnel FET

Tunnel FETs, also referred to as TFETs are the promising devices to replace the conventional MOSFETs for low power applications because of their quantum tunneling barrier. When the device is turned on, the carriers tunnel through the barrier in order for current to flow from source to drain. When the device is OFF, the presence of barrier keeps the OFF current extremely low which is several orders of magnitude lower as compared to the traditional MOSFET.

2.3.1 TFET structure and operation

The tunnel FET is a gated p-i-n device structure that is fully compatible with conventional MOSFET technology. Figure 2.6 shows the device structure utilizing a single gate.

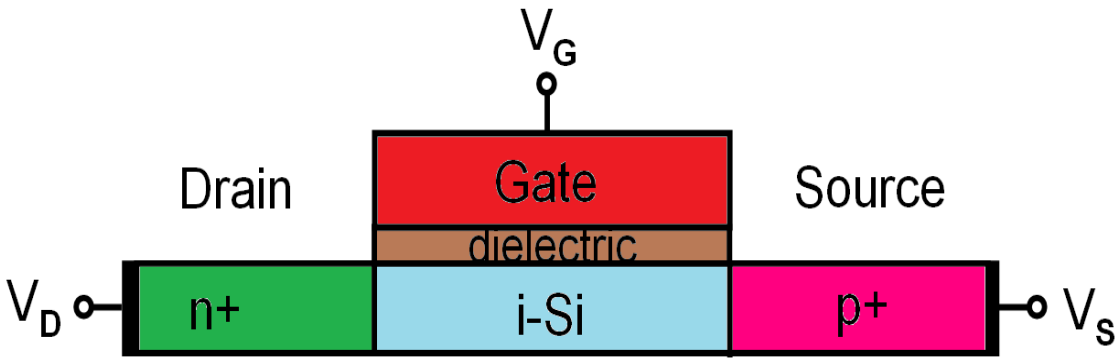

Figure 2.6: A simple TFET structure with one gate.

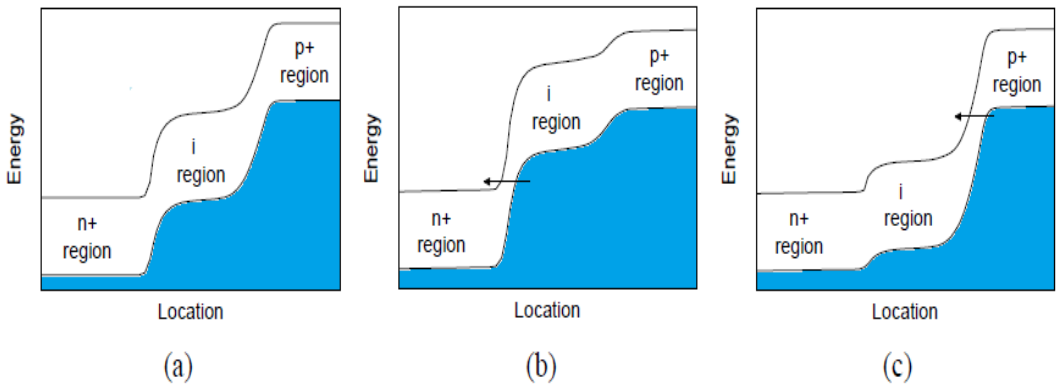

Figure 2.7: Energy band diagram of TFET. (a) off-state where the only current comes from p-i-n leakage, (b) on-state with a negative bias on the gate leading to pFET-type behaviour, and (c) on-state with a positive bias on the gate leading to nFET-type behaviour.

The regions in the tunnel FETs have been named as source, channel and drain respectively in order to be consistent with current MOS technology. The n(p) type device is turned OFF when the gate is held at 0V and turned ON when the positive (negative) voltage is applied to the gate. Source to drain junction is reverse biased in n(p) type device. The current conduction in TFET is through Band to Band Tunneling (BTBT). In n(p) TFET, electrons(holes) tunnel from source valence(conduction) band to drain conduction(valence) band.

When a Tunnel FET is designed with symmetry between the n- and p-sides (similar doping levels, similar gate alignment, etc.), the device exhibits ambipolar behavior, whereby the transfer characteristics resemble those of a pFET when a negative voltage is applied to the gate, and those of an nFET when a positive voltage is applied to the gate as shown in Figure 2.6.

2.3.2 Band-to-Band Tunneling (BTBT)

In TFETs, tunneling of interest is band-to-band tunneling. For band-to-band tunneling to occur, an electron in the valence band of semiconductor tunnels across the band gap to the conduction band without the assistance of traps. Leonid V. Keldysh and Evan O. Kane proposed models for the tunneling probability and the tunneling current (via BTBT) in semiconductors [29-30]. Equation 2.4 gives the tunneling current density for a direct bandgap material [31].

$$J_T = \frac{2\sqrt{2m^*}q^2F}{3\pi^3\hbar^2E_g^{1/2}}\exp\left[-\frac{\pi\sqrt{m^*}E_g^{3/2}}{2\sqrt{2}\hbar qF}\right] \quad 2.4$$

m^* is the carrier effective mass, F is the electric field, E_g is the semiconductor bandgap, and h is Planck's constant.

Equation 2.4 can be consolidated to give more common expression for Kane's equation as:

$$J_T = AF \cdot e^{-B/F} \quad 2.5$$

where A and B represent material properties for the semiconductor of interest. From equation 2.5, it can be seen that the BTBT generation rate of carriers into the channel is exponentially sensitive to the electric field at the tunneling junction which means that a larger electric field at the tunnelling junction produces a larger BTBT current (i.e., a larger I_{ON}). Therefore, while designing a TFET, one should incorporate a large built in electric field so as to increase I_{ON} and thus, the performance of a device for a given power supply. A conventional TFET design utilizes a very steep doping profile in the source in order to realize a large built-in electric field near the BTBT junction. Despite advancements in low energy ion implantation, flash annealing, and *in situ* doping during epitaxial growth, fabrication of very steep doping profiles remains a challenge. Conventional TFET, therefore, has the drawback of having low value of I_{ON} as compared to traditional MOSFET. Device engineers have come up with different ideas to enhance I_{ON} by incorporating double gate instead of single, using low band gap material, high K dielectric material or by using hetrostructures.

2.3.3 Subthreshold Slope of TFET

Subthreshold swing ('SS') is a quality measure of a device that determines the relationship between the subthreshold current and the gate voltage. It is defined as the amount of V_{GS} required to change the subthreshold current by an order of magnitude. A small 'SS' is preferred for higher ON current for a given OFF current value. The inverse subthreshold swing has a lower bound of 2.3 kT/q, or 60 mV/decade [32].From the definition of inverse 'SS', it can be also expressed as follows [32],

$$SS = \left(d\left(\log_{10} I_D\right) / \mathrm{dV_{GS}}\right)^{-1} \qquad 2.6$$

The dependence of subthreshold swing on gate voltage is shown in Figure 2.8 [33]. Two important observations can be drawn. First, the subthreshold swing of TFETs is not constant, but rather a function of gate voltage. Secondly, at low gate voltages, it is possible for Tunnel FETs to have a subthreshold swing less than the 60 mV/decade MOSFET limit at room temperature. When the subthreshold swing is calculated as in equation 2.6' the result is [34]:

$$SS = \log_{10}\left[\frac{1}{V_{eff}}\frac{d_{Veff}}{d_{VGS}} + \frac{F+b}{F^2}\frac{dF}{dV_{GS}}\right]^{-1} \qquad 2.7$$

Where, V_{eff} is the bias at the tunnel junction and F is the electric field at the tunnel junction.

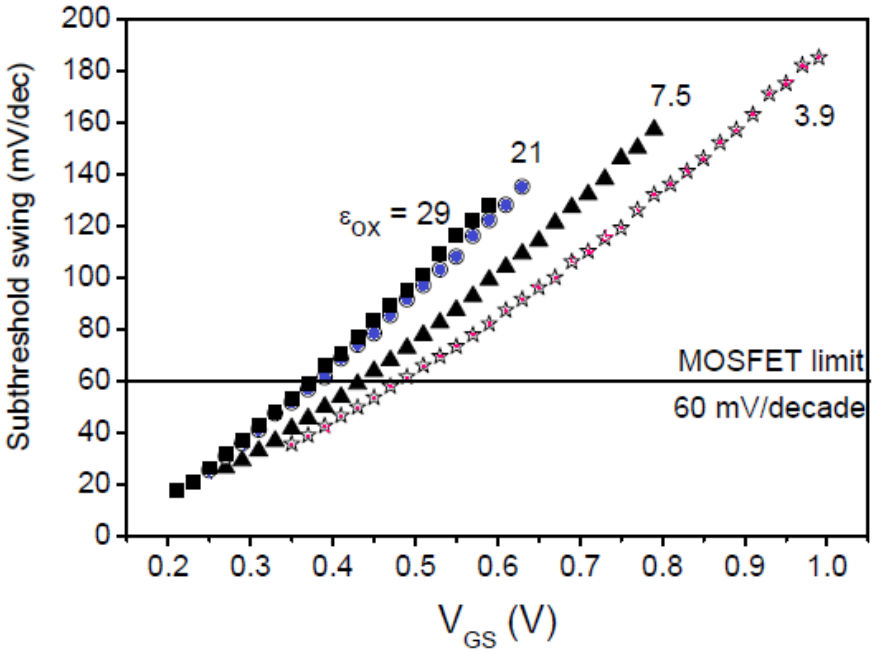

Figure 2.8: Tunnel FET subthreshold slope dependence on gate voltage for different dielectric constants [33].

$$b = 4\sqrt{m^*}Eg^{3/2} \Big/ 3q\hbar \qquad 2.8$$

From equation 2.7, it should be noted that the the subthreshold swing is a function of V_{GS} which is in sharp contrast with conventional MOSFET. This means that the subthreshold region does not appear as a straight line when I_{DS}-V_{GS} is plotted on a log-linear scale, and the swing does not have one unique value. Swing is smallest at the lowest V_{GS}, and increases as V_{GS} increases. Thus, a steep subthreshold swing allows low power operation of device as power scales as the square of V_{DD}. A steep SS device requires less gate voltage for a given I_{ON}/I_{OFF} ratio. Therefore, the research on TFETs seeks to reduce power dissipation while maintaining the performance of a given system.

2.3.4 State-of-the-art of the TFET

The first investigation containing the basic element of tunnel transistor was conducted by Stuetzer in 1952 [35]. He showed the ambipolar nature of the current–voltage *I–V*, in the field gating of a lateral Ge p–n junction. Quinn et al. at Brown University [36] were the first to propose the gated p-i-n structure of a Tunnel FET in 1978, and suggested the usefulness of this device for spectroscopy. They proposed the formation of a surface-channel MOS tunnel junction by replacing the n-type source of an n-MOSFET with a highly degenerate p type source. In 1988, Leburton *et al.* [37] proposed the first vertical TFET with the aim of creating a high-speed transistor in which the gate was used to control the negative differential resistance (NDR). Baba [38] in 1992, fabricated Tunnel FETs which he called Surface Tunnel Transistors, using MBE in III-V materials. In 1994, Reddick and Amaratunga proposed and fabricated the first known Si based BTBT transistor [39]. They were motivated by the desire for devices that would be faster than conventional MOSFETs, as tunneling devices are, and that could be scaled down more easily without running into problems such as punchthrough. Hansch *et al.* [40] in 2000 proposed and fabricated a Si vertical TFET and noted its potential for low off-current relative to the MOSFET. In 2004, Aydin *et al.* [41] fabricated Lateral Interband Tunneling Transistors on SOI. These devices used a different TFET structure without an intrinsic region and placing the gate over a p-n junction. They claimed that this would reduce gate capacitance and therefore increase speed. They also claimed that there should be no current saturation for these devices. In 2004, the concept of low subthreshold swing in TFET was reported by wang [42], Bhuwalka [43], and Appenzeller [44]. A subthreshold swing smaller than the 60 mV/dec limit of conventional MOSFETs was reported for the first

time by [44]. [43] proposed a Tunnel FET on silicon with a SiGe delta layer, grown by molecular beam epitaxy "MBE". The SiGe replaced the silicon delta layer so that the smaller bandgap should have reduced the tunnel barrier width and increased tunneling current in the on-state as well as lowering the subthreshold swing. Boucart *et.al* [45], showed that length scaling in nanometers dimensions gives much better results as compared to MOSFET. TFET, unlike MOSFET, does not suffer from SCE, DIBL and have much better I_{ON} / I_{OFF} ratio and sub-threshold swing is not limited by temperature. It can, therefore, be much lower than 60mV/dec even at room temperature and will have much lower sub-threshold power consumption, that might be very useful for low power/sub-threshold region applications. The same author in [46] has shown ways to boost up the ON current of silicon TFET, using double gate structures to double the ON current and utilizing high K dielectrics. To further enhance the ON current, Ge material [47] is employed.

We have published an optimized TFET paper which will be covered in chapter 5.

2.4 Introduction to Carbon Nanotube Field Effect Transistor (CNFET)

Carbon Nanotubes field effect transistor (CNFET) is one of the most promising device that could eliminate most of the fundamental limitations of traditional silicon devices. Improved channel transport and high carrier velocity of CNT results in significant improvement in speed over Si MOSFET [48, 49, 50]. They have the potential to minimize the subthreshold slope (i.e., minimize the short channel effects). Initially there was lot of fabrication issues with CNFET technology. However, most of these issues like positioning and alignment of CNTs along with the presence of metallic CNTs have been solved [51, 52]. Moreover, CNFET can be fabricated using the existing CMOS technology infrastructure and it can also be integrated with CMOS on the same chip [53], therefore, most of the fabrication issues have been solved and CNFET holds a bright future and a lot of promise. This section briefly introduces CNFET technology.

2.4.1 Carbon Nanotubes

The carbon nanotube is made by rolling up a sheet of graphite or graphene (a monolayer of sp^2 bonded carbon in a honeycomb lattice, which are even stronger than the sp^3 bonds in diamond) into a cylinder. This makes atomic electromigration more

difficult which means that carbon nanotubes are an extremely stable structure that avoids damage from high currents [54]. These cylindrical carbon tubes have remarkable electrical properties, which are valuable for nanotechnology, electronics, optics, and other fields of material science and technology. Nanotubes are categorized as single walled CNTs (SWCNTs) and Multi walled CNTs (MWCNTs).

Carbon nanotubes (CNTs) are hollow cylinders of graphene having varying diameter (0.4nm to 4nm) and it provides a single path between source and drain. They can be classified depending upon the direction in which the graphene sheets are rolled up either as semiconducting with distinct band gap or metallic with no band gap. The resulting structure is called single-walled carbon nanotube (SWCNT). If more than one SWCNT of varying diameters are folded concentrically, they form a multi walled CNT (MWCNT). The properties of CNTs such as bandgap, conductivity, diameter etc. are determined by its chirality (n_1, n_2). A SWCNT works as metal if $n_1 = n_2$ or $n_1 - n_2 = 3i$, where 'i' is an integer. Otherwise, it works as a semiconductor. The relationship between chirality (*Ch*), CNT diameter (D_{CNT}) and threshold voltage (V_{th}) is given by:

$$Ch = a\sqrt{(n_1^2 + n_2^2 + n_1 n_2)} \tag{2.9}$$

$$D_{CNT} = Ch / \pi \tag{2.10}$$

$$V_{th} \approx \frac{E_g}{2} = \frac{aV_\pi}{qD_{CNT}\sqrt{3}} \tag{2.11}$$

Where *Eg* is the energy gap, *q* = electronic charge, $a = \sqrt{3}d$ = 2.49Å is the lattice constant (where d = 1.44 Å is the inter-carbon-atom distance) and V_π =3.033eV is the carbon π–to–π bond energy in the tight bonding model [55, 56].

The working principle of CNFET is similar to that of conventional MOSFET. The bulk semiconductor channel is replaced by a number of semiconducting carbon nanotubes as shown in Figure 2.9. Since the carriers are now confined to a narrow nanotube, their mobility increases due to quasi 1-D (ballistic) transport.

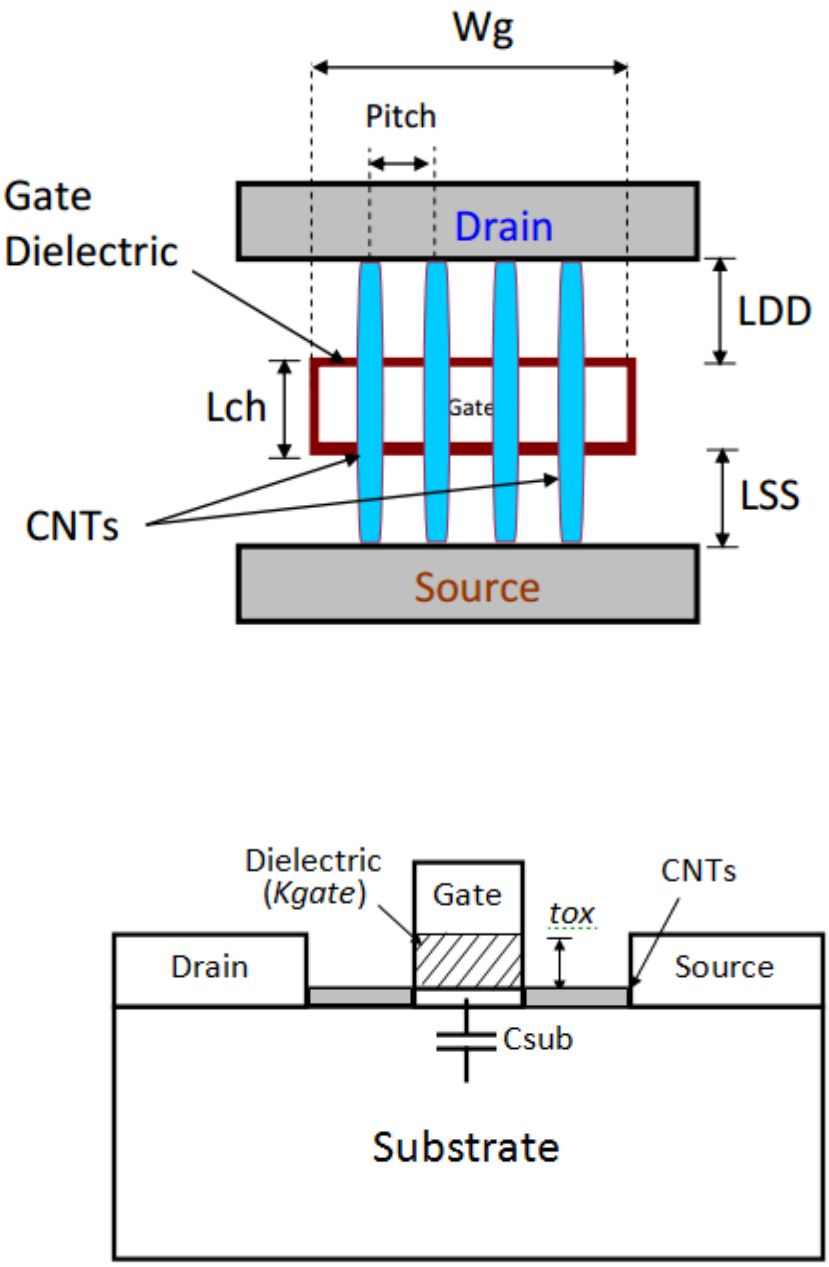

Figure 2.9: Carbon Nanotube Field Effect Transistor.

2.4.2 CNFET Model Overview

A circuit-compatible CNFET model from Stanford University is used for the simulation purpose [49] [57]. It provides improved accuracy by accounting for several practical non-idealities, such as scattering, effects of the doped source/drain extension region, and inter-CNT charge screening effects. In addition, by including a full trans-capacitance network, it does better predictions of the dynamic performance and transient response.

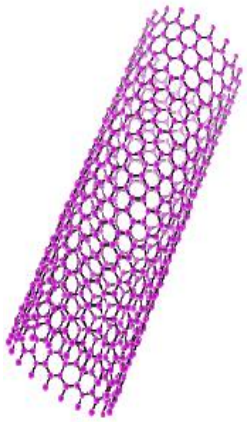

Figure 2.10: Structure of SWCNT.

The semiconducting intrinsic CNT, shown in Figure 2.10, under the gate acts as the channel and heavily doped CNT regions outside the gate forms the source/drain extension regions.

The model is organized hierarchically into three levels [58] as shown in Figure 2.9. The first level (L1) describes the intrinsic CNT region that forms the channel under the gate. Several non-idealities, such as near ballistic transport and parasitic components are taken into account here. For a MOS-like n-type CNFET, the hole current is usually negligible as compared to the electron current for semiconducting sub-bands. This is due to heavily doped source/drain extension regions (n-type). The opposite is true for p-type CNFETs.

The second level L2 represents the heavily doped source/drain extension region and takes into account the effects such as elastic scattering, parasitic resistances of the source/drain extension region, parasitic capacitances of the source/drain extension region, and the Schottky barrier resistance of the source/drain metal contacts.

The third level L3 models the effects such as CNT-to-CNT charge screening and the gate-to-neighboring-contact parasitic capacitances. Practical CNFETs must contain multiple CNTs per device in order to achieve sufficient drive current at reasonable speed. Thus, the model allows multiple nanotubes and accounts for the CNT-to-CNT charge screening effect present in this device. In other words, CNTs only experience charge screening from their immediate neighbors.

2.5 Summary

This chapter has successfully introduced the concept of technology scaling that result in faster and smaller transistors to achieve higher performance and higher chip density but static power consumption issues increase significantly. Hence, increased leakage power dissipation becomes a major bottleneck while designing low power circuits for portable application. This chapter also presents an overview of promising emerging devices. It explains the need for alternative technologies like TFETs and CNFETs and also reviews their basic concepts.

The next chapter explores CMOS device optimization to achieve better subthreshold slope and I_{ON}/I_{OFF} ratio to enhance the speed and to reduce the switching energy of subthreshold circuits.

CHAPTER 3

Optimization and Characterization of CMOS for Ultra Low Power Applications

Chapter 3

OPTIMIZATION AND CHARACTERIZATION OF CMOS FOR ULTRA LOW POWER APPLICATIONS

In the subthreshold regime, the aggressive voltage scaling holds great challenges and promise for strict energy budget applications. It has been established, however, that high speed superthreshold devices are not suitable for moderate performance subthreshold applications. The selection of threshold voltage (V_{th}) and oxide thickness (T_{OX}) is much more flexible for subthreshold applications rather than superthrehold one at low voltage levels. It is therefore, necessary to explore and optimize silicon MOSFET's process and geometry parameters at Nano technological node. This chapter calibrates the process and electrical parameters for n and p type MOS with 35nm physical channel length. Subsequently, the calibrated MOS device for superthreshold application is optimized for better performance under subthreshold conditions using Synopsys Technological Computer Aided Design (TCAD) simulation. The simulated device shows 9.89% enhancement in subthreshold slope and 34% benefit in I_{ON} / I_{OFF} ratio for the same drive current.

3.1 Introduction

CMOS technology scaling trends are mostly concentrated on achieving higher speed. Device fabrication process parameters selection for Ultra Low Power (ULP) applications with lower operating voltages and frequencies is still under exploration [10, 59-62]. It has been shown in [61] that subthreshold circuit performances are significantly gained by optimizing the device geometry parameters. For superthreshold circuit applications, process and geometry parameters are largely dictated by different leakage currents and, hence, severely affect its static power dissipation [32, 63-66]. However, due to lower bias supply, gate leakage current, DIBL, and punchthrough effects are almost negligible under subthreshold conditions [24]. Therefore, it seems to some extent that the design constraint for selecting V_{th} and T_{OX} are more flexible in subthreshold region of operation.

scaling of V_{th} for superthrehold devices, is limited by the amount of static leakage, mainly subthreshold leakage current in submicron technology nodes [60, 61]. A high V_{th} device will give notable performance penalty under subthreshold conditions due to lower subthreshold leakage current. Therefore, the choice of V_{th} is a tradeoff between speed and leakage power dissipation in case of superthreshold applications. However, in subthreshold region, lower static leakage power dissipation due to scaled V_{DD} even below V_{th} allows further reduction in V_{th} to enhance the speed of subthrehold devices and circuits

Gate leakage along with subthreshold leakage is also a major bottleneck in aggressive T_{OX} Scaling in order to obtain better control over the channel for superthreshold devices [60, 61]. T_{OX} generally scales down from 130 nm technology in case of high frequency applications to keep gate leakage minimum due to higher bias [60]. However, it degrades subthreshold slope (SS). In subthreshold regime due to lower V_{DD}, T_{OX} reduction will not significantly increase the gate leakage current [24]. Moreover, transistor input capacitance is smaller under subthreshold conditions than the superthreshold region of operation [61]. Therefore, more aggressive T_{OX} scaling is possible to achieve higher speed and lower power consumption under subthreshold regime.

Halo and retrograde doping are generally needed to suppress short channel effects in case of superthrehold devices in submicron technology. These doping wells are used to reduce Drain Induced Barrier Lowering (DIBL) and punch through effects and to control V_{th} of the device independent of its subthreshold slope. However, due to lower bias in subthreshold region, DIBL and punch through effects are not significant at all. Therefore, subthreshold device characteristics are less sensitive to halo and retro doping. This chapter, therefore explores the subthreshold design of MOS device at 45nm technology node with enhanced subthreshold slope and higher current drive capability of the device.

3.2 Calibration of MOS Device

As shown in Figure 3.1, L_g and T_{OX} of the device are set as the transistor's performance parameters [67]. In [68], authors have fabricated the optimized 35nm gate length NMOS device at V_{DD} = 0.85V with 676 $\mu A/\mu m$ drive current capability, subthreshold slope = 86mV/dec., and I_{OFF} = 100nA/μm. The said device is fully

optimized for short channel effect (SCE) suppression and parasitic resistance reduction.

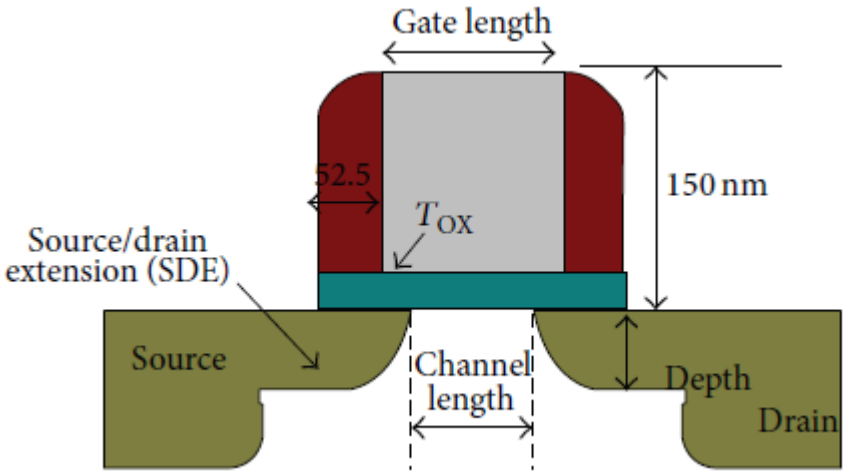

Figure 3.1: CMOS Device structure.

There is a need to design a superthreshold device with better performance at 45nm technology node. Then it can be optimized to get an optimum subthrehold device. For this purpose, NMOS device is fabricated in [68].The physical dimensions of a 35nm device are listed in Table 3.1 [68]. The poly-Si thickness is 150 nm, while the distance of S/D contact to gate is 52 nm. Source and drain contactss are treated as ohmic for simulation purpose. The resulting SDE junction depth is 15nm for NMOS and 28nm for PMOS. Lower T_{OX} for PMOS causes more drive current in PMOS comparable to NMOS. Also, lower T_{OX} of PMOS will cause more vertical electric field in channel which further increases the subthreshold drive capabilities in PMOS. Moreover, channel and halo doping are tuned to calibrate our device with the fabricated NMOS device in [68] and its corresponding electrical characteristics are listed in Table 3.2. To begin with, the simulation project is accurately matched with the process details of real structure by incorporating the physical parameters given in Table 3.1. The calibrated 45nm device structure is obtained as shown in Figure 3.2.

(I_{DS}-V_{GS}) and (I_{DS}-V_{DS}) characteristics are the primarily set as a target for calibration in device simulation. The calibration begins by adjusting the electrostatic in order to match subthreshold slope, drain current, and I_{OFF}. Finally, device measurements are tuned and matched to the calibrated device [68] by doping profiles adjustment in order to obtain the desired *I-V* characteristics. The flowchart depicting the calibration

process is shown in Figure 3.3 [69]. Tuned mobility parameters are used for process calibration.

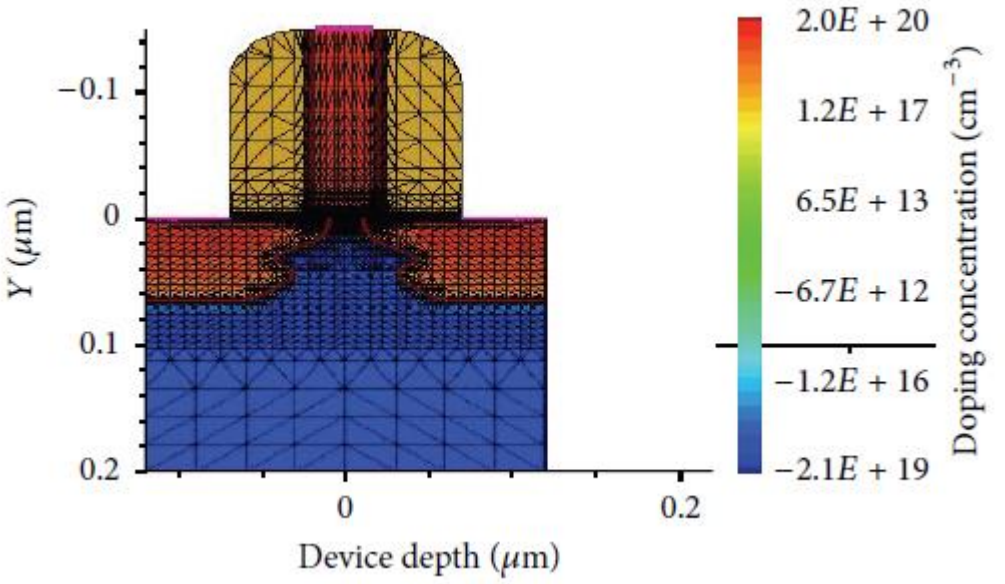

Figure 3.2: Meshed structure of 45 nm NMOS.

The matched calibrated electrical characteristics are obtained through Synopsys TCAD simulation utilizing Sentaurus workbench. The significant figures of merit, thus, extracted from simulation, are then compared with the experimental data given in Table 3.2. This marks the beginning of investigating the effect of physical and process parameters under subthreshold conditions.

Table 3.1: Device geometry for 35 nm channel length MOS Device [68].

	Gate length (nm)	**T_{OX} (nm)**	**Junction Depth (nm)**	**Poly silicon thickness (nm)**	**Spacer thickness (nm)**
NMOS	35	1-1.2	20	150	52.5
PMOS	35	0.95	33	150	52.5

Table 3.2: Performance Parameter listing of Simulated Device with experimental one.

	[68]		This work (simulation)	
	NMOS	**PMOS**	**NMOS**	**PMOS**
I_{ON} (μA/μm)	676	272	676	300
I_{OFF} (nA/μm)	100	100	106	110
SS (mV/dec)	86.1	92.3	83.88	90.56

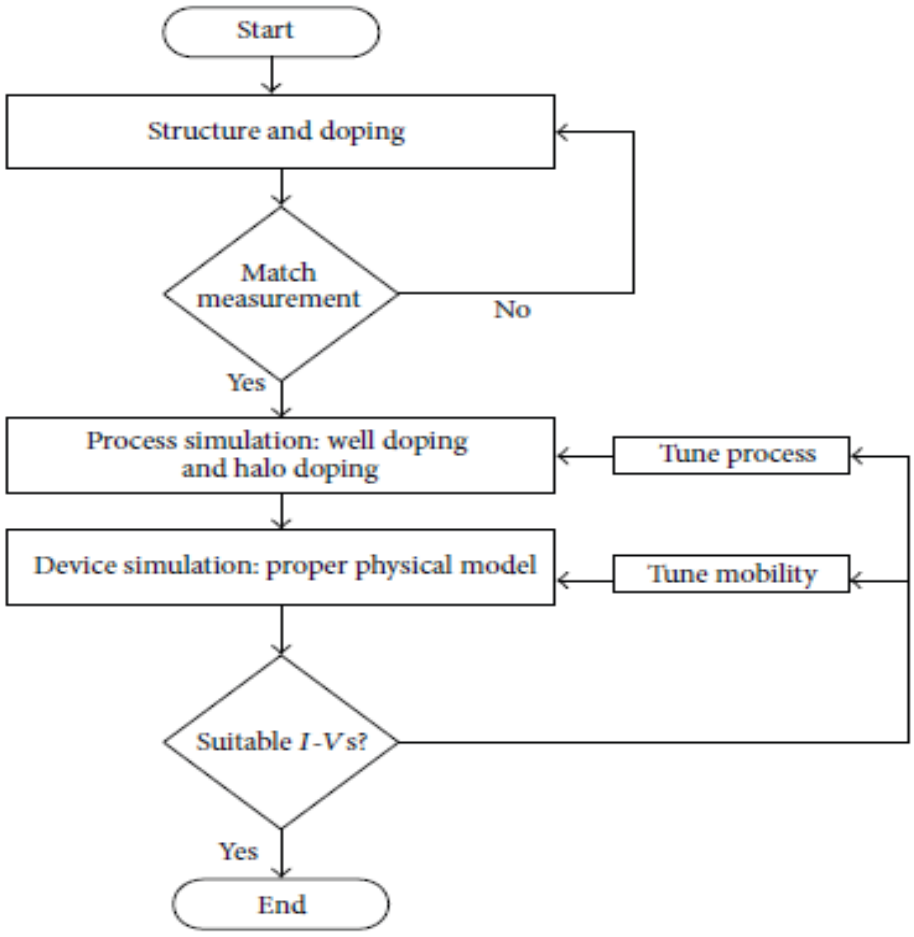

Figure 3.3: Flowchart depicting calibration methodology [64].

3.3 Oxide and Channel Length Variations effects under subthreshold Condition

One of the key techniques to enable gate length scaling is to scale T_{OX} [70]. Therefore, T_{OX} scaling has been influential in controlling SCEs as MOS device dimensions get reduced. This improves the control of the gate electrode over the channel. As depicting in Figure 3.4, as T_{OX} scales down, there is a marked increase in gate leakage

current which becomes significant below 65nm technology node. Moreover, gate capacitance also increases significantly with T_{OX} scaling for superthreshold devices and circuits. In order to reduce the gate leakage, a gate dielectric with higher dielectric constant k is introduced below 45 nm [71]. Due to lower supply voltage V_{DD}, gate leakage component, however is negligible under subthreshold as compared to superthreshold region of operation.

As shown in [72], the effective gate capacitance C_g of a transistor is largely dominated by intrinsic depletion and parasitic capacitances that are strongly dependent on T_{OX} variations.

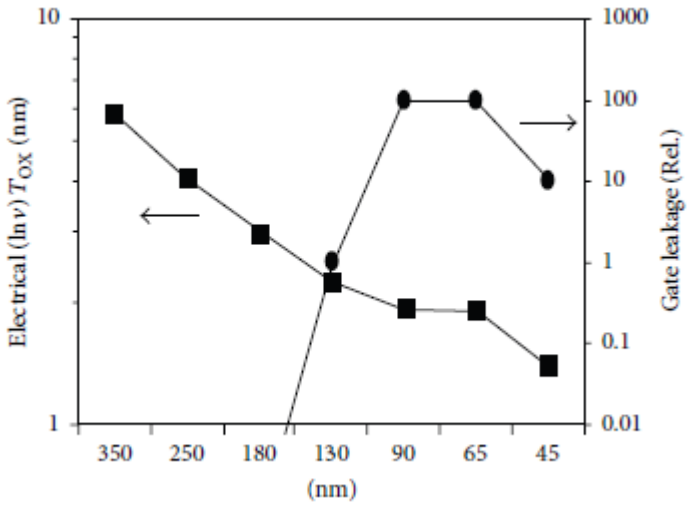

Figure 3.4: T_{OX} scaling and gate leakage versus Intel technology [10].

In power constraint subthreshold design of circuits, devices are normally optimized to enhance the speed [73, 74]. Reduction of capacitances can be achieved by using higher value of T_{OX}. This, however results in the reduction of the gate control over the channel. Moreover, it results in higher value of SS. Therefore, for moderate speed applications with little bit loss of energy, remarkable improvement in speed can be achieved. furthermore, under subthreshold conditions with (V_{GS} < 0.3), T_{OX} scaling does not increase gate capacitance C_g significantly contrary to superthreshold region of operation as shown in Figure 8.5. The effective channel length also regulates subthreshold leakage current and V_{th}. Hence, this part of the section examines the combine effect of T_{OX} and L_g scaling on the performance of the device. As shown in Figure 3.2, the calibrated NMOS device, is simulated to explore the joint impact of L_g and T_{OX} on the NMOS device characteristics under subthreshold conditions at V_{DD}

=150mV. Variations in the values of L_g and T_{OX} are carried out from 30 nm to 50 nm and 0.6nm to 1.3nm respectively, whereas the values of halo and substrate doping are kept constant at 1.6e+19/cm^3 and 2.2e+18/cm^3, respectively. It can be deduced from Figure 3.6 that with an increase in L_g and a decrease in T_{OX}, significant reduction in SS is observed. With the increase in L_g from 35 to 50 nm SS reduces by approximately 6mV/decade for different values of T_{OX}. As seen from Figure 3.7, an increase in channel length has a minimal effect on the gate capacitance. Hence, longer channel length will result in lower power dissipation and better performance due to improved SS. Moreover, reduction in the value of T_{OX} from 1 to 0.8 nm at L_g = 35nm reduces SS by 2.3mV/decade and an increase in C_g by 12%. Therefore, careful selection of T_{OX} is required so that the improvement in SS will not be masked by an increase in C_g and therefore, the power dissipation ($C_gV_{DD}^2f$). It is obvious from Figure 3.7, that T_{OX} is having a larger impact on C_g as compared to L_g. furthermore, it can be observed that with an increase in L_g ,I_{ON} and I_{OFF} reduces by 14x and 22x, respectively, at T_{OX} = 1 nm. Accordingly, I_{ON} /I_{OFF} ratio increases by 1.36x at T_{OX} =1 nm with the corresponding increase in L_g. This also helps in the reduction of power consumption. Optimum value of L_g can be obtained from Figure 3.8, for better values of SS and I_{ON} /I_{OFF} ratio for various values of T_{OX}. From the above investigation, it can be deduced that, for energy efficient ULP circuits and systems, larger value of L_g can be used to reduce the energy consumption due to smaller SS and higher I_{ON} /I_{OFF} ratio. Nevertheless, for high performance ULP applications, an increase in L_g will appreciably reduce the drive current and therefore the speed of the operation of the circuit. Hence, larger values of L_g are not feasible for high performance ULP applications.

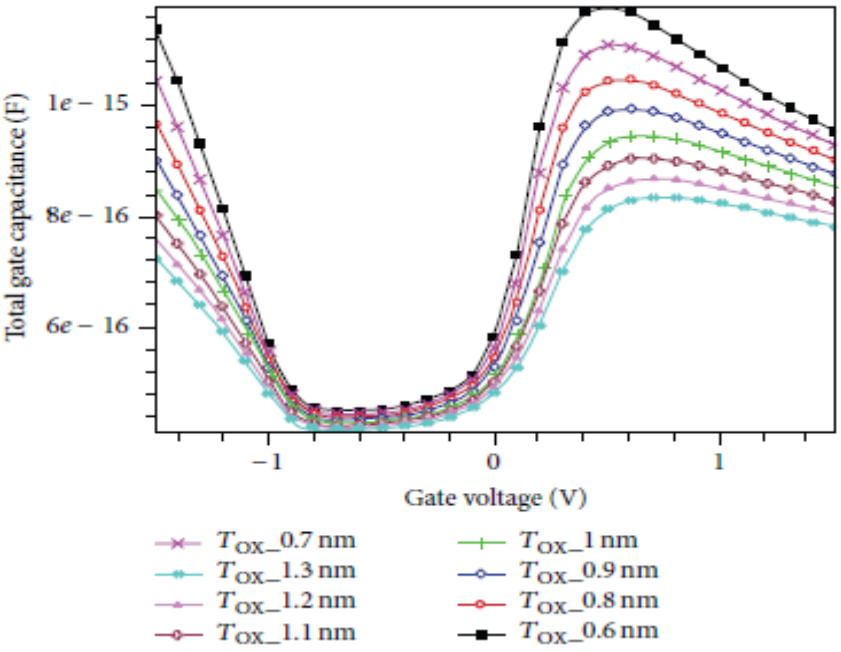

Figure3.5: Gate capacitance variation with V_{GS} for 45 nm NMOS.

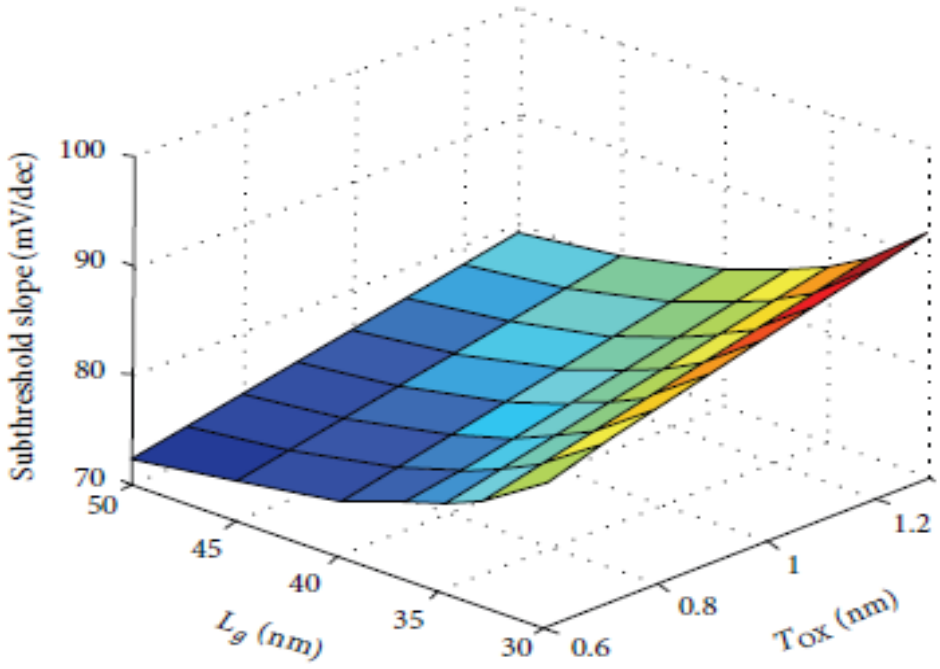

Figure 3.6: Subthreshold slope variation with L_g and T_{OX} for 45 nm NMOS.

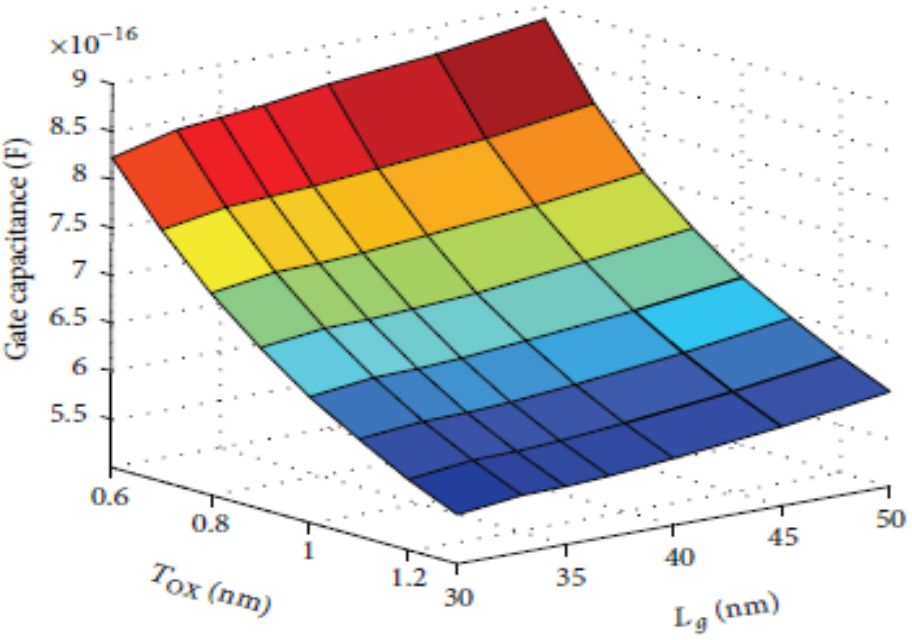

Figure 3.7: Gate capacitance variation with L_g and T_{OX} for 45 nm NMOS.

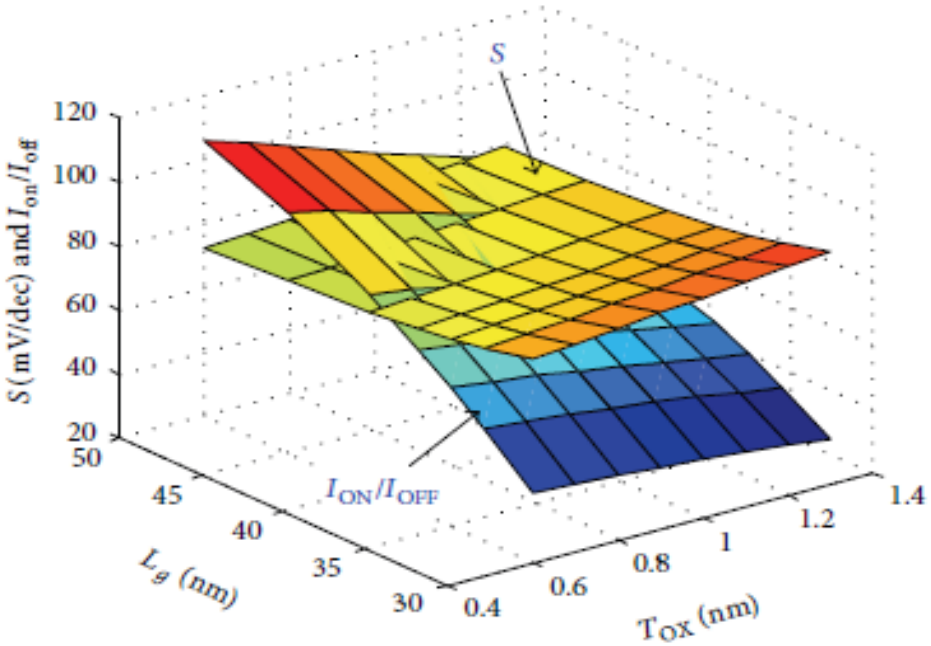

Figure 3.8: Subthreshold slope and I_{ON}/I_{OFF} variations with L_g and T_{OX} for 45 nm NMOS.

3.4 Doping Profile Variation Effects under Subthreshold Condition

It has been observed that in scaled superthreshold devices, halo and retrograde doping are used to suppress short channel effects (SCE) like DIBL and punchthrough effect [75]. Nevertheless, in subthreshold region, SCE plays a least significant role as compared to superthreshold region because of lower values of V_{DD} [24]. Therefore, it has now been well established that halo and retrograde doping profiles are less significant under subthreshold regime. Furthermore, low doping profile levels can reduce the junction capacitance significantly. Hence, it is essential to explore the effect of doping profile under subthreshold conditions in nanometer technology nodes.

It can be observed from Figure 3.9 that with the reduction in substrate *(N_{sub})* and halo doping, there is an appreciable increase in the drain current *(I_{sub})*. The decrease in N_{sub} doping concentration by 50% increases I_{sub} by 3.5x. Moreover, reducing N_{halo} by 4x increases I_{sub} by 2.25x. However, from Figure 3.10, it can be deduced that with the reduction in N_{sub} by 50%, there is an increase in SS by 0.7mV/decade and I_{OFF} by 3.88x. Hence, there is a trade-off involved in boosting the drive current, SS and I_{OFF} on reducing N_{sub} doping concentration. Similar observable trends in performance are observed by varying the halo doping concentration. Figure 3.11 and 3.12 exhibit the drain current *(I_{sub})* and subthreshold slope (SS) as a function of halo and substrate doping.

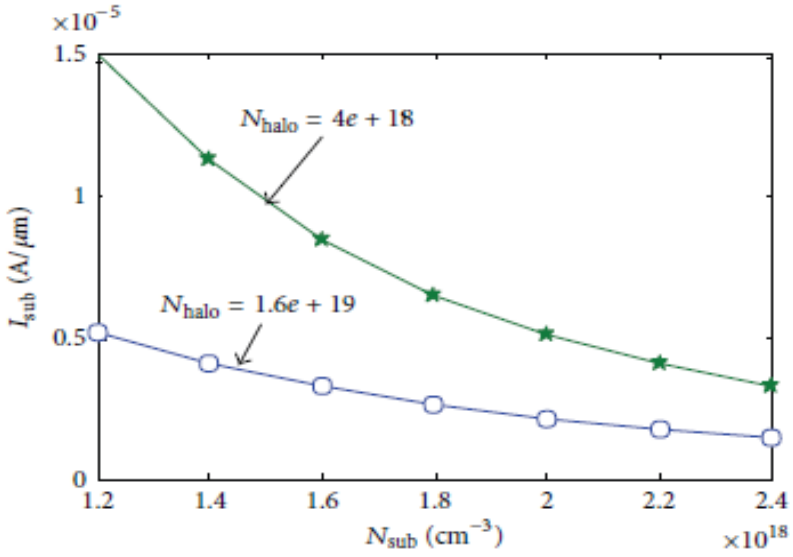

Figure 3.9: Drain current variation with channel doping for different halo dose.

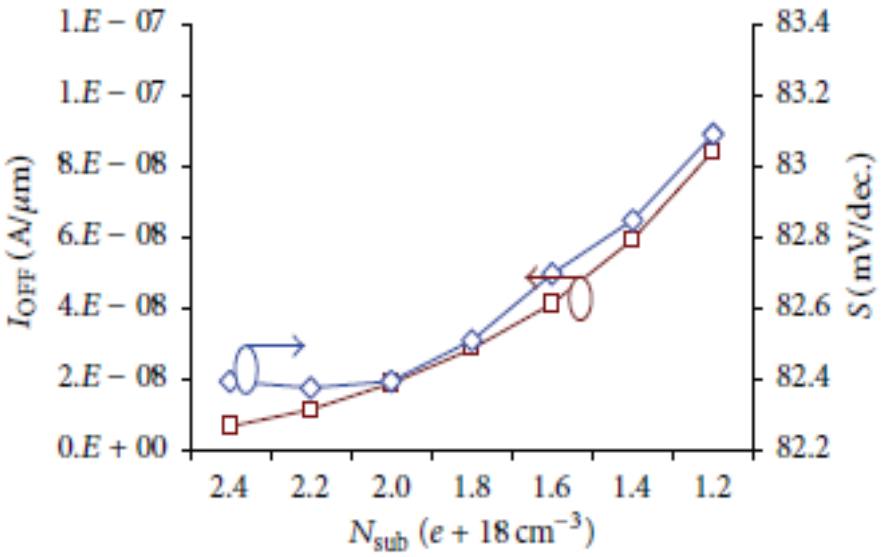

Figure 3.10: Subthreshold slope and I_{OFF} variation with channel doping.

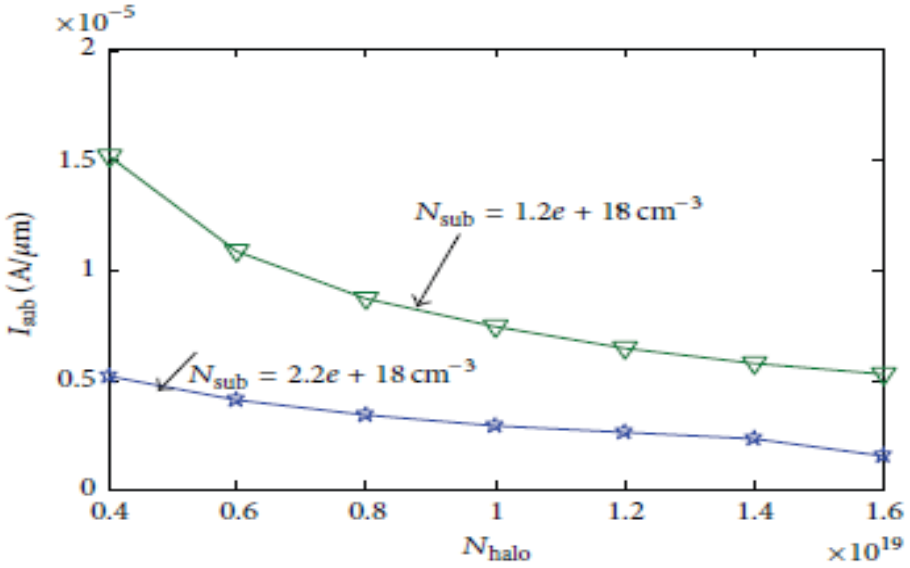

Figure 3.11: Drain current variation with halo doping.

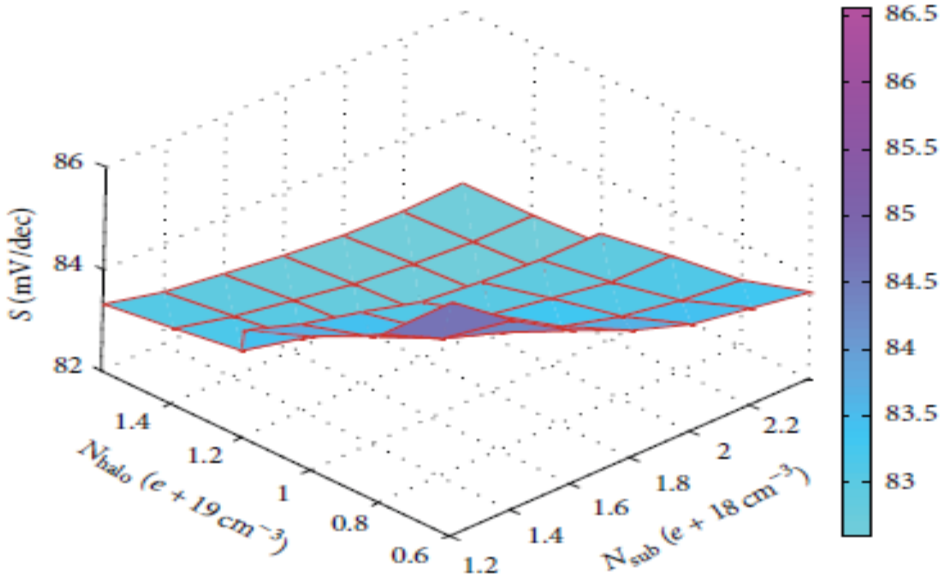

Figure 3.12: Subthreshold slope variation with halo doping and channel doping.

3.5 Characterization of Device under Subthreshold Condition

This section deals with the subthreshold slope improvement so that power consumption can be reduced [24]. The calibrated device is then fine-tuned at optimum values of L_g, T_{OX}, N_{sub} and N_{halo} in order to achieve best subthreshold characteristics. Optimized device parameters from Section 3.4 are used to achieve better subthreshold slope under subthreshold conditions. Figure 3.13 shows the comparison of the subthreshold slope as a function of supply voltage for the standard and the optimized device under subthreshold condition.

As depicted in Figure 3.13, the optimized device showed a marked improvement of 9.89% in subthreshold slope over the traditional device operated in subthreshold region. Moreover, as depicted in Table 3.3, I_{ON}/I_{OFF} ratio increases by 34% in case of optimized device for the same drive current. Since the effect of DIBL is very negligible under subthreshold conditions, therefore this work does not taken into account the DIBL effect during device optimization.

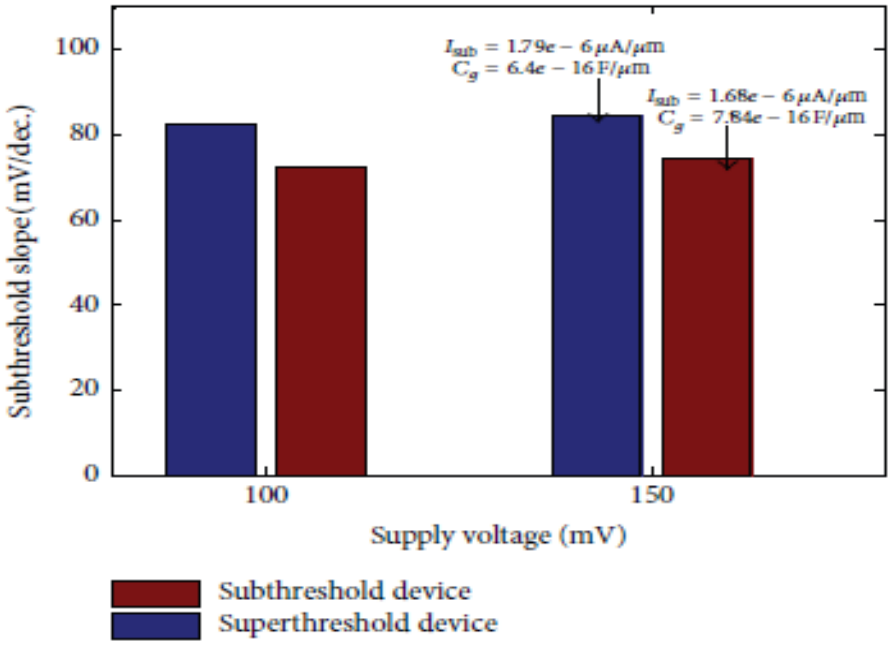

Figure 3.13: Subthreshold slope Versus supply voltage.

Table 3.3: Performance parameter comparison under subthreshold conditions.

	[68]	**This work (simulation)**
I_{ON} (µA/µm)	1.79	1.68
I_{OFF} (nA/µm)	32	19.9
SS (mV/dec)	82.58	74.41

3.6 Summary

The device designed particularly for superthreshold region of operation is not worthy for optimum subthreshold region. This chapter proposed new device process parameters in order to improve the subthreshold slope and to enhance the speed of subthreshold devices and circuits. It has successfully presented the optimized device for subthreshold region which results in improvement in both the subthreshold slope and the I_{ON}/I_{OFF} ratio. Therefore, in order to obtain the better device performance characteristics under subthreshold conditions, it is necessary to optimize the process and geometry parameters of Silicon MOSFET at nanometer technology node due to the relaxed constraint for different leakage currents and short channel effects.

The next chapter presents the design and optimization of ultra-low power CMOS based second generation current conveyor (CCII) in the subthreshold region at 32nm technology node. Optimal sizing of transistors for different designs has been done at low supply voltages.

CHAPTER 4

Subthreshold Design of Second Generation Current Conveyor

Chapter 4

SUBTHRESHOLD DESIGN OF SECOND GENERATION CURRENT CONVEYOR

Current mode circuits like current conveyors have attained significant importance especially in the field of current analog ICs design as compared to their voltage mode counterparts due to higher speed, lower power consumption and lesser chip area. This chapter presents the design and optimization of ultra low power second generation current conveyor (CCII) in the subthreshold region. Optimal sizing of transistors for different designs has been done at low supply voltages ranging from ±0.7V to ±0.25V. A design operating at supply voltage of ±0.25V and bias current of 20pA was found to be optimal. HSPICE simulations were performed to measure various performance parameters of CCII at the 32nm technology node.

4.1 Introduction

4.1.1 Importance of Ultra Low Power Design

Ultra-low-power (ULP) design is important for biomedical systems because biomedical implants should be small, consume minimum power and dissipate minimum heat. A fully implanted system with a battery that has a limited number of wireless recharges must operate under stringent low-power constraints such that constant surgery is not needed to change the battery in a patient. Thus, ULP operation will always be paramount in implantable biomedical systems [76]. ULP demands that the transistors should operate in the subthreshold regime where the supply voltage is lower than the threshold voltage of a MOS transistor.

4.1.2 Subthreshold operation of a MOS transistor

In subthreshold regime, the drain current in a MOSFET is given by

$$I_D = I_0 \frac{W}{L} e^{\frac{V_{gs}-V_{th}}{nV_t}} (1-e^{-V_{ds}/V_t}) \tag{4.1}$$

where I_0 is the technology dependent subthreshold current extrapolated for, $V_{gs} = V_{th}$, $V_t = kT/q$ is the thermal voltage, W/L is the aspect ratio and 'n' is the subthreshold factor [77]. The operation of a MOS device in subthreshold region is necessary for ultra low power circuits [78]. A whole class of CMOS circuits has been developed for the weak inversion operation of MOS device [79]. The MOS device can be used to achieve higher gain in subthreshold region as I_D is exponentially dependent upon V_{gs}. But the speed of subthreshold circuits is severely limited because of large device sizes and low drain current [80]. It is possible to operate devices at quite low voltages in the range of 0.25-0.3V without sacrificing their functionality in subthreshold regime that reduces power consumption at the cost of reduced speed.

There is a need of a basic building block that can be used to implement large number of different analog functions and that too in the subthreshold region. Second generation current conveyor (CCII) can be regarded as a real competitor for the operational amplifier (OPAMP). The classical OPAMP has suffered from constant gain band-width product problem and has low slew rate at its output. It has unreliable frequency response and remains unsatisfactory for high frequency applications. CCII, being a current mode device, has larger dynamic range, higher band-width, greater linearity, simpler circuitry, lower power consumption, and reduced chip area as compared to their voltage mode counterparts like Operational amplifiers. Due to its flexibility and versatility, CCII finds applications in realizing impedance convertors, integrators, differentiators, filters etc. [81-84]. Few low voltage CCII structures have been reported so far operating at a supply voltage of 1V or less but they are unable to meet ultra low power constraint on account of their complex structure [85-87]. Current conveyor structures, characteristics and performance have been investigated in [88, 89] in super-threshold region but to the best of our knowledge its design, performance and characteristics have not yet been explored under subtreshold condition. Hence, this chapter investigates, for the first time, the design and optimization of a CCII under subthreshold condition.

The rest of the chapter is organized as follows. A brief introduction of CCII is given in section 4.2. Section 4.3 and 4.4 deal with the design and performance analysis of various parameters of CCII for different designs. In section 4.5, Monte Carlo variability analysis of optimal design is done followed by the design of an

instrumentation amplifier based on the designed CCII in section 4.6. Section 4.7 then summarizes the chapter.

4.2 Basics of Second Generation Current Conveyor

The first generation current conveyor was introduced by Sedra and Smith in 1968. Later in 1970, they came up with a novel type of current conveyor known as second generation current conveyor [90, 91]. Second generation current conveyor (CCII) is basically a versatile current mode (CM) device which conveys current with unity gain from the input port to the output port. With one high input impedance, one low input impedance and one high output impedance, it is a suitable element for both voltage-mode and current-mode circuits and can be used to perform many useful functions. The block diagram representation of CCII and its internal transistor implementation are shown in Figures 4.1 and 4.2 respectively.

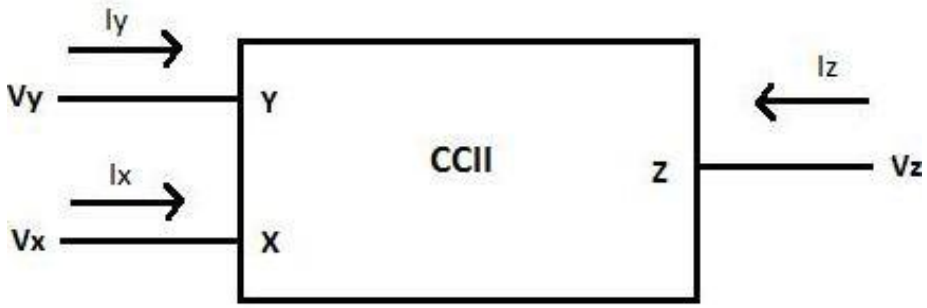

Figure 4.1: CCII block diagram.

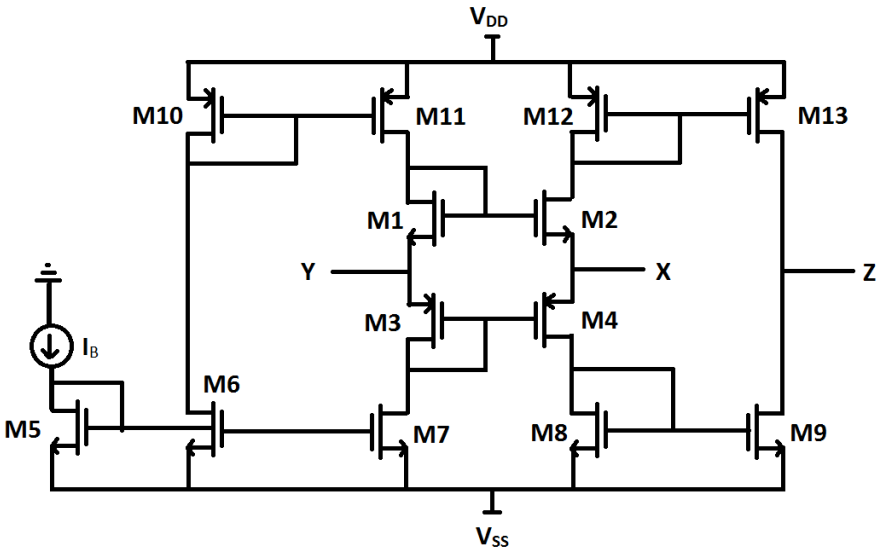

Figure 4.2: CMOS based circuit of CCII.

The characteristic equations of the dual output current conveyor can be represented as follows:

$$\begin{aligned} I_Y &= 0 \\ V_X &= V_Y \\ I_Z &= \pm I_X \end{aligned} \qquad 4.2$$

where V_X and V_Y are the voltages at ports X and Y, respectively. I_X and I_Y are the currents entering ports X and Y. Moreover, I_{Z+} is the positive-type output current and I_{Z-} is the negative type output current. Ideally, a current conveyor should satisfy the following conditions:

1) Infinite input impedance (R_Y) at port Y.

2) Zero input impedance (R_X) at port X for current inputs.

3) Infinite output impedance (R_Z) at port Z.

4) Unity current transfer gain between ports X and Z.

5) Unity voltage transfer gain between ports Y and X.

6) Infinite bandwidth

4.3 CCII Structures and Design Considerations

Figure 4.2 uses a mixed translinear loop (transistors M1–M4) as the input of the CCII. Transistors M5, M7 and M10, M11 form two current mirrors that allow the mixed loop to be dc biased by the current. The input transistors present high input impedance at port Y and a low impedance at port X. This configuration acts as a voltage follower. The output Z copies the current flowing through port X and is realized in the conventional manner using two complementary mirrors as current follower.

The following section presents the design of a translinear loop based CCII in the subthreshold regime. The critical issue in designing translinear based CCII structure in the superthreshold region is the matching of NMOS and PMOS loop components in which μ_n and μ_p are process dependent parameters [89]. The situation becomes more critical in subthreshold region especially for submicron devices. Considering the various trade off conditions, different designs of translinear CCII structures are

simulated using PTM 32nm level-54 model [92]. The performance evaluation of each design is carried out on the basis of various key characteristics of CCII namely current gain (α), voltage gain (β), current bandwidth, voltage bandwidth, resistances and their respective bandwidths at various ports of CCII.

4.3.1 Design of classic translinear structure

The design begins by transistor sizing on the basis of mobilities of NMOS and PMOS transistors [88, 93]. The adjusted aspect ratios of different transistors in [88] and [93] are such that will keep all the transistors in the saturation region and they utilize 0.35 µm and 0.25 µm CMOS process parameters respectively. The optimal sizing of each transistor in this design of the current conveyor is done according to [88] and [93] using 32nm technology node. The supply voltage and bias current are adjusted such that all the transistors operate in the subthreshold region ($V_{gs} < V_{th}$). The aspect ratios of the transistors are listed in Table 4.1.

Table 4.1: Transistors channel widths and lengths

Transistor	W/L
M1-M2	1.28µm / 0.064µm
M3-M4	2.048µm / 0.064µm
M5-M9	0.768µm / 0.064µm
M10-M13	1.28µm / 0.064µm

The supply voltage is varied from ±0.7V to ±0.3V and the bias current is also changed for a particular supply voltage keeping all the transistors in the subthreshold region. All simulations are performed using HSPICE and performance parameters variations are plotted in Figures 4.3-4.9. Table 4.2 lists the performance parameters at ±0.3V supply voltage and at a bias current of 5nA and is compared with [88].

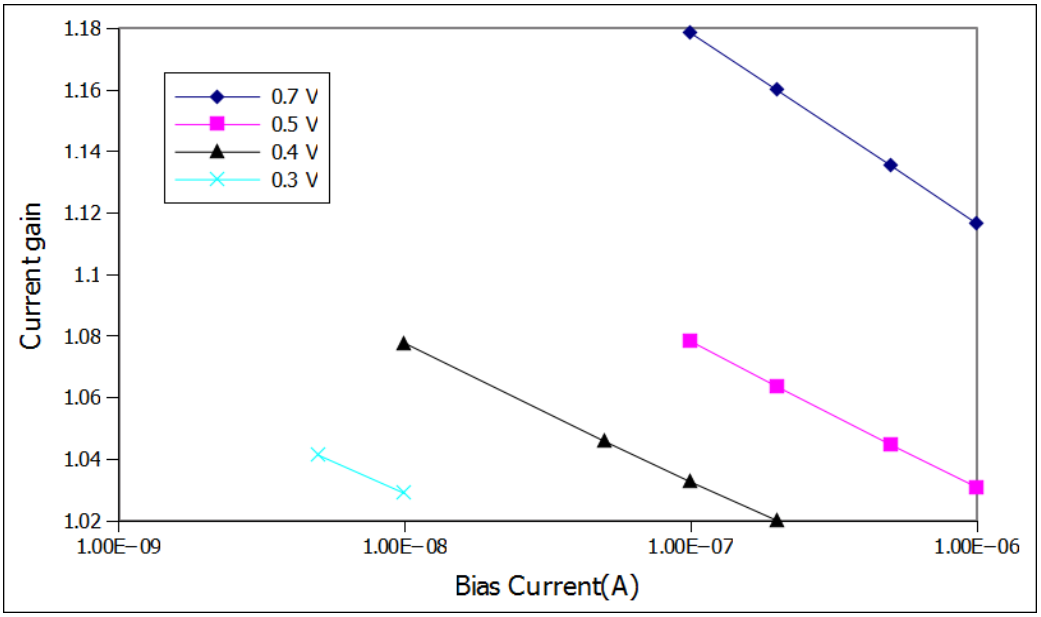

Figure 4.3: Plot of current gain Vs bias current for various biasing supply.

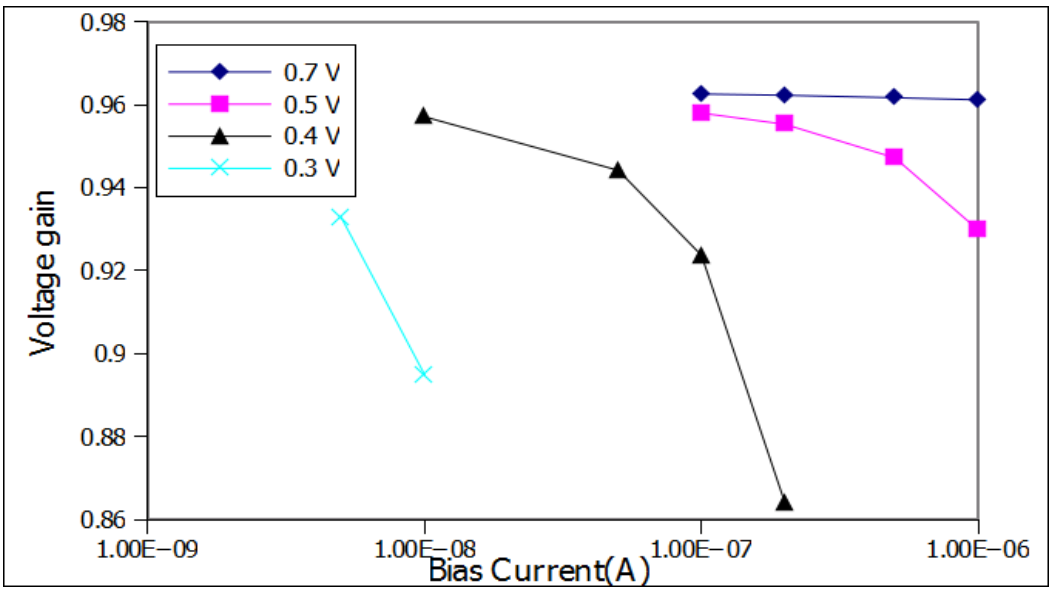

Figure 4.4: Plot of voltage gain Vs bias current for various biasing supply.

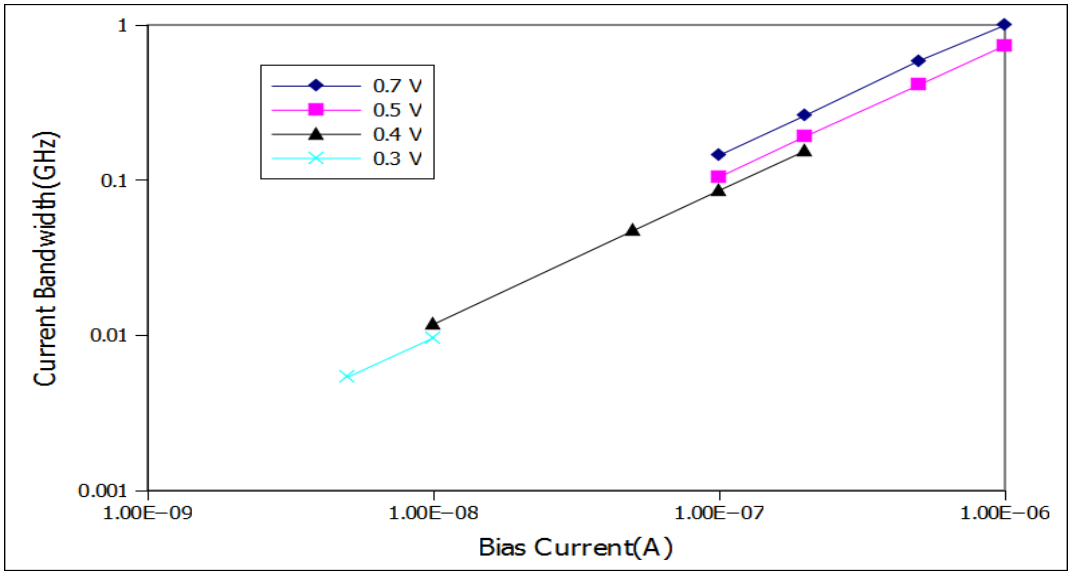

Figure 4.5: Plot of current bandwidth Vs bias current for various biasing supply.

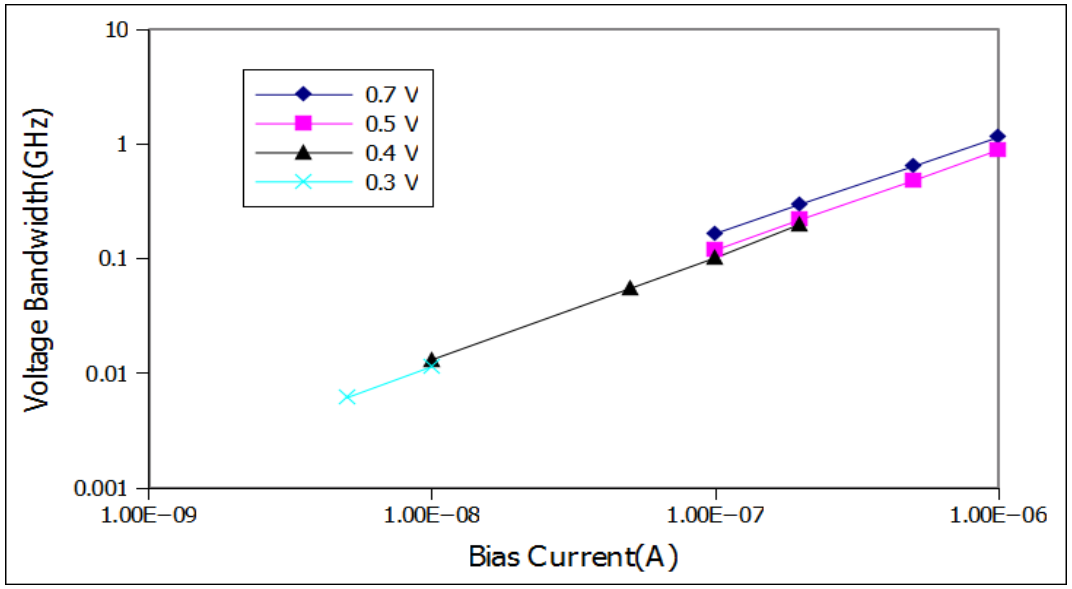

Figure 4.6: Plot of voltage bandwidth Vs bias current for various biasing supply.

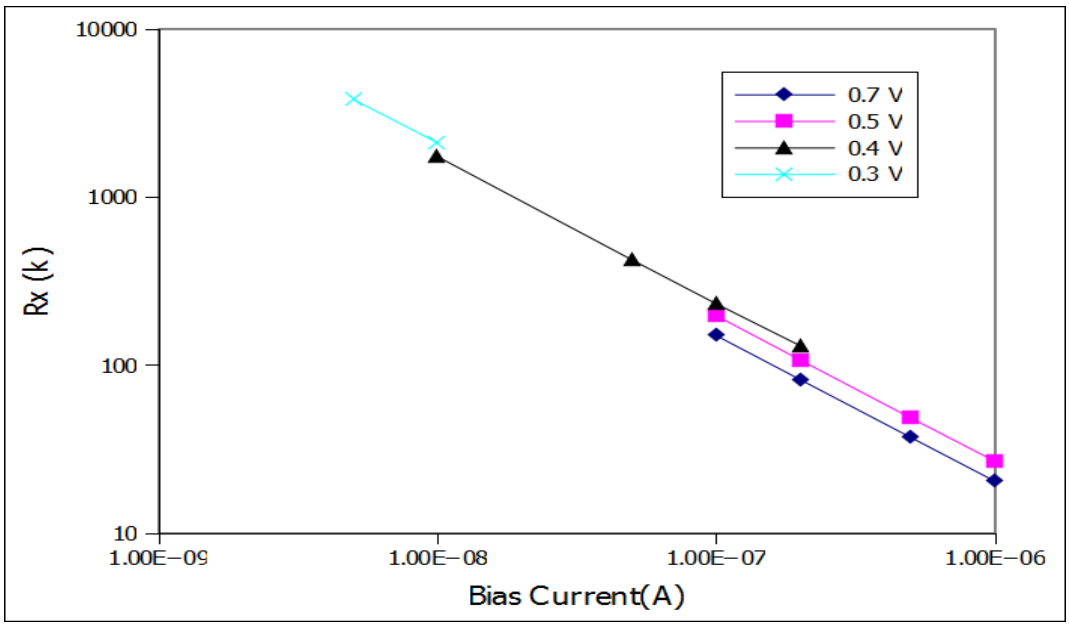

Figure 4.7: Plot of input impedance (R_X) Vs Bias current for various bias supply.

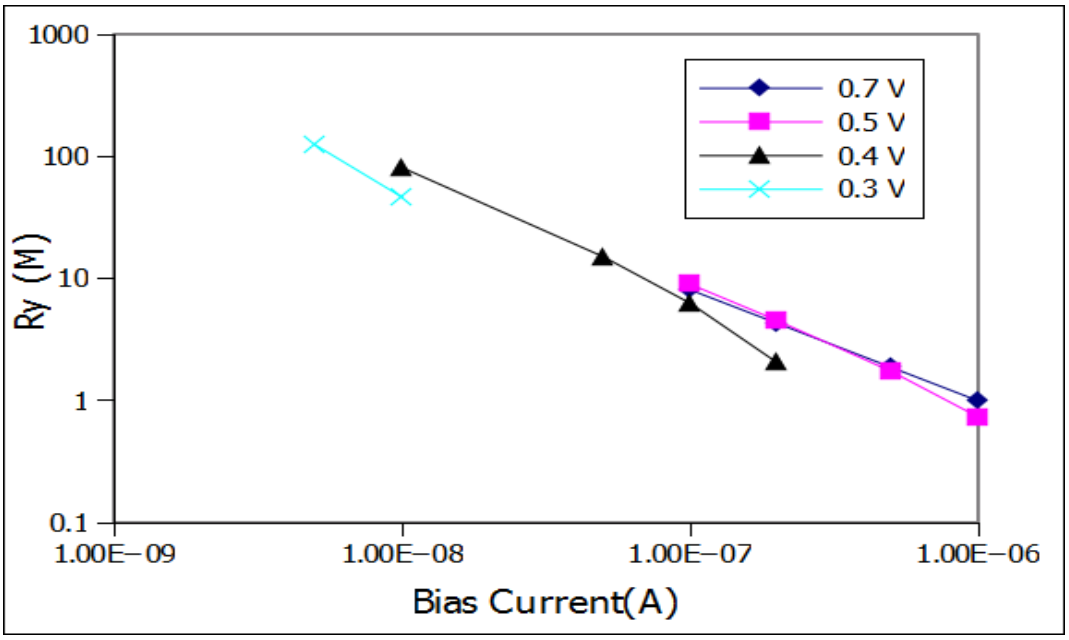

Figure 4.8: Plot of input impedance (R_Y) Vs Bias current for various biasing supply.

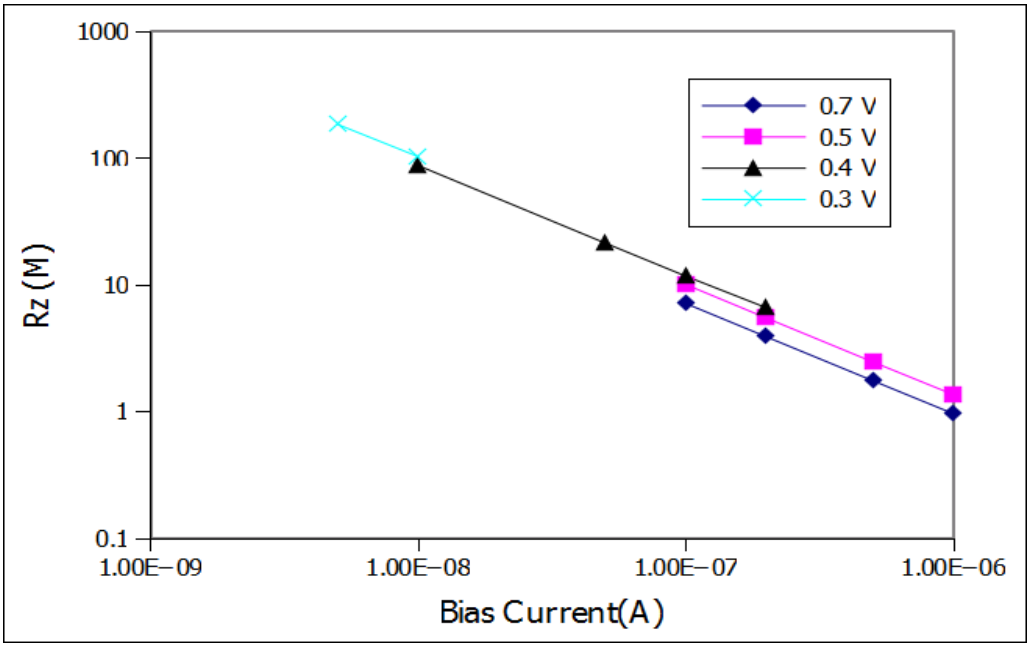

Figure 4.9: Plot of output impedance (R_Z) Vs Bias current for various bias supply.

Table 4.2: Performance Parameters of CCII

Parameters	[88]	This Design
V_{DD}	±1.5 V	±0.3 V
I_B	50 µA	5 nA
α	1.02	1.0413
β	0.9515	0.9328
α-3dB (MHz)	393	5.38
β-3dB (MHz)	503	6.14
R_X	1.44 kΩ	3.81 MΩ
R_Y	37.54 kΩ	124.06 MΩ
R_Z	197.1 kΩ	185 MΩ
3dB R_X (MHz)	-	18.7
3dB R_Y (MHz)	-	0.182
3dB R_Z (MHz)	-	0.374

It can be observed from Table 4.2 that as the supply voltage and bias currents are reduced, there is a significant reduction in power dissipation as the transistors are moved into the subthreshold region at the cost of reduced bandwidth and higher port resistances. However, there is a considerable current mismatch in the current mirror as we move deep into the subthreshold region by reducing the bias current and supply voltage due to drain induced barrier (DIBL) lowering as explained in the next section.

4.3.2 Subthreshold Current Mirrors

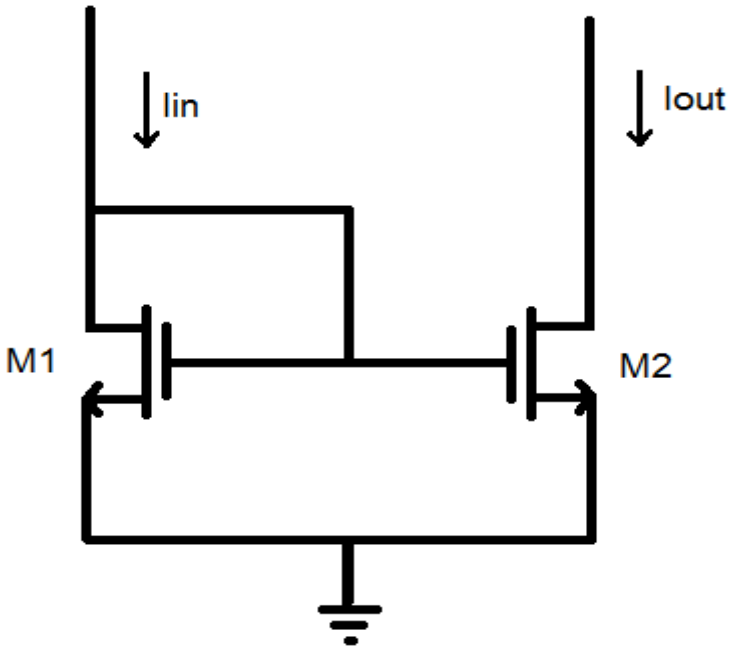

Figure4.10: Basic Current Mirror circuit.

By using equation 1, the ratio of drain currents of M1 and M2 can be written as follows:

$$\frac{I_{out}}{I_{in}} = \frac{I_0(\frac{W}{L})_2 e^{\frac{V_{gs2}-V_{th2}}{nV_t}}(1-e^{-V_{ds2}/V_t})}{I_0(\frac{W}{L})_1 e^{\frac{V_{gs1}-V_{th1}}{nV_t}}(1-e^{-V_{ds1}/V_t})} \qquad 4.3$$

If both transistors have the same aspect ratio and $V_{ds} > 4V_t \approx 100\text{mV}$, then $(1-e^{-V_{ds}/V_t})$ ≈ 1, and hence, the above equation can be re-written as:

$$\frac{I_{out}}{I_{in}} = \frac{e^{\frac{V_{gs2}-V_{th2}}{nV_t}}}{e^{\frac{V_{gs1}-V_{th1}}{nV_t}}} \tag{4.4}$$

In equation 1, the threshold voltage V_{th} also depends on the drain-source voltage V_{ds} (through the drain induced barrier lowering (DIBL) effect) and the bulk-source voltage V_{bs} (through the body effect) according to:

$$V_{th} = V_{th0} - \lambda_{ds} V_{ds} - \lambda_{bs} V_{bs} \tag{4.5}$$

Where $\lambda_{ds} > 0$ is the DIBL coefficient and $\lambda_{bs} > 0$ is the body effect coefficient [94].

Since $V_{gs1} = V_{gs2}$ and source and body are at same potential, so, $V_{bs} = 0$ hence the above equation reduces to,

$$\begin{aligned} \frac{I_{out}}{I_{in}} &= e^{\frac{V_{th1}-V_{th2}}{nV_t}} \\ \frac{I_{out}}{I_{in}} &= e^{\frac{\lambda_{ds}(V_{ds2}-V_{ds1})}{nV_t}} \\ \frac{I_{out}}{I_{in}} &= e^{\frac{\lambda_{ds}\Delta V_{ds}}{nV_t}} \end{aligned} \tag{4.6}$$

Where $\Delta V_{ds} = V_{ds2} - V_{ds1}$

Hence, current mismatch in subthreshold current mirror is exponentially dependent on drain to source voltage mismatch.

The expressions for the current gain (α) and voltage gain (β) is given as follows [95] :

$$\alpha = \frac{I_z}{I_x} = \frac{g_{m2}g_{m8}g_{m13} + g_{m4}g_{m9}g_{m12}}{g_{m8}g_{m12}(g_{m2} + g_{m4})} \tag{4.7}$$

$$\beta = \frac{V_X}{V_Y} = \frac{g_{m2} + g_{m4}}{g_{m2} + g_{m4} + (r_{ds2})^{-1} + (r_{ds4})^{-1}} \tag{4.8}$$

It can be deduced from Figure 4.3 that for a particular supply voltage as the bias current increases, current gain tends towards unity. When the bias current increases,

drain to source voltage mismatch of current mirrors reduces and hence from equation 4.6, current mismatch also reduces. Thus, current gain comes closer to unity.

Figure 4.4 shows the variation of the voltage gain with the bias current and the trends are just the reverse of Figure 4.3. For a constant supply voltage, if bias current increases then the deviation of the voltage gain from unity increases. As bias current increases, drain to source resistances r_{ds} reduces and hence from equation 4.8, voltage gain β deviates away from unity with β<1. It is possible to find the optimum supply voltage and bias current by the intersection of current and voltage gains curves which gives least possible deviations in current gain and voltage gain. Figures 4.5-4.6 show the variation of the voltage and the current bandwidths with the bias current respectively. Simulation results indicate that both the 3-dB current and voltage bandwidths decrease as the bias current and supply voltage reduce. The observed reduction in the bandwidths is due to the lower value of transconductance at lower current/voltage levels**.** Furthermore, it is observed from Figures 4.7-4.9 that the resistances at ports X, Y, and Z increase in a similar manner on the reduction of bias current and supply voltage due to lower current level. The observed trends indicate that an optimum supply voltage and bias current have to be investigated to achieve optimum performance of a CCII.

4.4 Non-Minimal length designs of CCII

This section investigates different designs by incorporating non-minimal length of transistors and various performance parameters have been evaluated keeping all the transistors in the subthreshold regime. The various designs and their aspect ratios are listed in Table 4.3. To begin with, aspect ratios of M5-M9 (NMOS) are chosen depending upon silicon area consumption allowance. Depending on the μ_n/μ_p ratio of 32nm technology, aspect ratios of M10-M13 (PMOS) are chosen to be 3.5 times that of M5-M9. For M1-M2 and M3-M4, aspect ratios are chosen to be 1.5 times of M5-M9 and M10-M13 respectively. Design 1 to Design 4 follows the same procedural steps of choosing the aspect ratios of various transistors. As shown in Table 4.3, aspect ratios of M5-M9 are subsequently scaled down from 5 to 0.25 from Design 1 to Design 4.

Table 4.3: W/L ratios of different designs

	M1-M2	**M3-M4**	**M5-M9**	**M10-M13**
Design 1	7.5	26.25	5	17.5
Design 2	3	10.5	2	7
Design 3	0.75	2.625	0.5	1.75
Design 4	0.375	1.3125	0.25	0.875

The supply voltage is varied from ±0.3V to ±0.25V and bias current is varied from 750pA to 20pA for different designs. As one moves from design 1 to design 4, significant reduction in power consumption is obtained, resistances at Y and Z terminal change from tens of gigaohms to hundreds of gigaohms while resistance at X terminal also increases from tens of megaohms to around thousands of megaohms. This increase in resistance R_x is due to the inverse dependence of resistance on the bias current [96]. Current and voltage bandwidths lie in the range of hundreds of kilohertz which is suitable for biomedical applications. The lengths of transistors have to be non-minimal in subthreshold design to reduce current mismatch. For this reason, lengths of the transistors have been taken five to six times of L_{min}, which ensures that the currents mismatch is within ±10% limit on account of high output resistance.

Table 4.4: Performance parameters for different Designs.

		Design 1 $L=5L_{min}$	**Design 2 $L=5L_{min}$**	**Design 3 $L=5L_{min}$**	**Design 4 $L=5L_{min}$**	**Design 4 $L=6L_{min}$**
1	V_{DD} (V)	±0.3	±0.3	±0.3	±0.3	±0.25
2	I_B (pA)	750	250	100	30	20
3	α	1.0107	1.0106	1.0100	1.0100	1.002
4	β	0.9830	0.9845	0.9812	0.9824	0.9722
5	α-3dB (KHz)	331	282	437	281	138
6	β-3dB (KHz)	510	437	666	428	234
7	R_X (M)	23.63	69.76	182.49	588.22	887.52
8	R_Y (G)	3.096	9.263	21.2232	69.54	72.48
9	R_Z (G)	4.080	7.09	32.5	85.1	113
10	Current deviation	±7.5%	±9.8 %	±5%	±9.66%	±8.9 %
11	Area (μm^2)	3.040	1.664	0.416	0.208	0.299

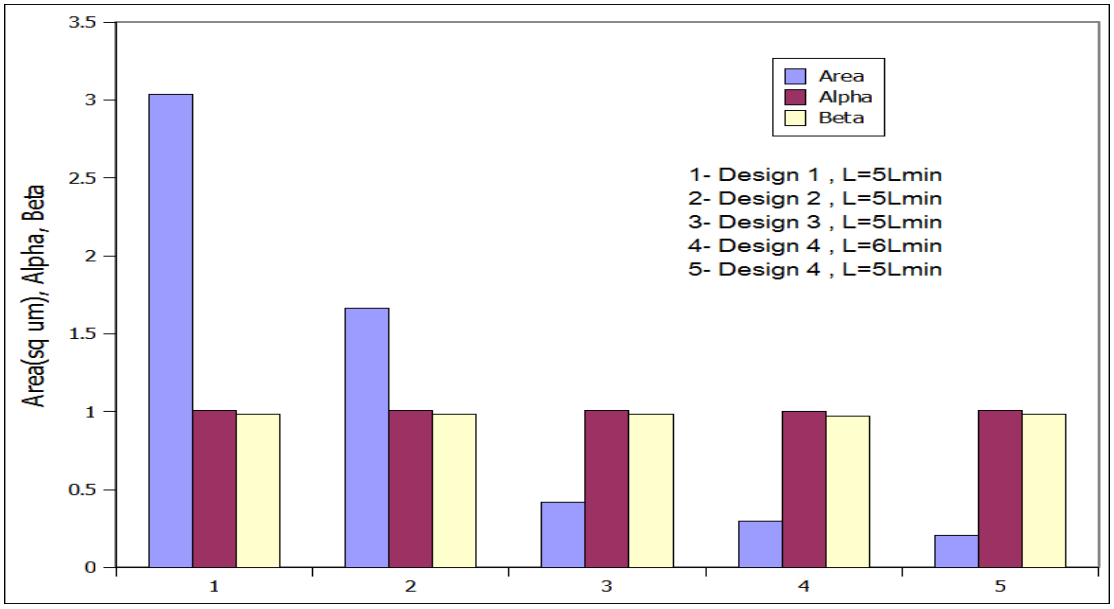

Figure 4.11: Variation of area, current and voltage gain for different designs.

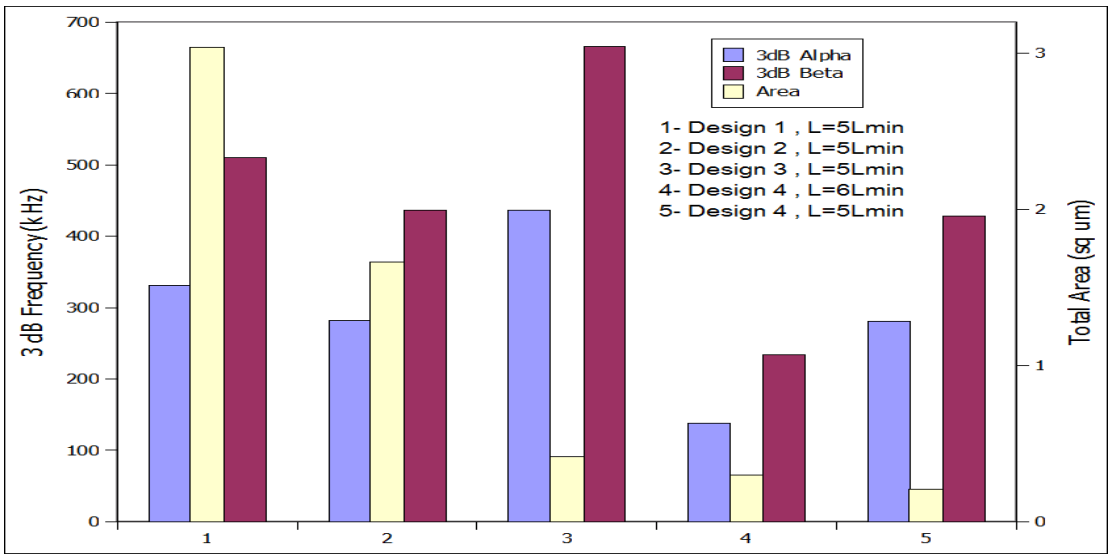

Figure 4.12: Variation of area, current and voltage gain 3dB frequency for different designs.

The variation of different performance parameters of CCII with total area of the device for each design is shown in Figures 4.11-4.13. It can be deduced from Figure 4.11 that as the total area increases, voltage and current gains follow same trends of approaching unity. For a particular design (4,5 in Figure 4.11), if we increase area by increasing the lengths of the transistors, then current and voltage gains come closer to unity. From Figure 4.12, it is obvious that if area increases for a given design (4, 5 in Figure 4.12) then voltage and current bandwidths decrease because of the increase in device capacitances. Figure 4.13 shows that if area reduces then resistances seen by different ports increase. Thus, we can see that for Design 4 having $L=5L_{min}$, the area is minimum. But in this design two transistor's widths come out to be less than $1.5L_{min}$. In order to ensure that the width of each and every transistor is at least $1.5L_{min}$, Design 4 having $L=6L_{min}$ is taken into consideration. It can be operated at 20pA bias current and at even lower supply voltage of ±0.25 V. The power dissipation for this particular design is also minimum and it shows better trade off in performance parameters amongst all the implemented designs, thereby, making it the most optimal design.

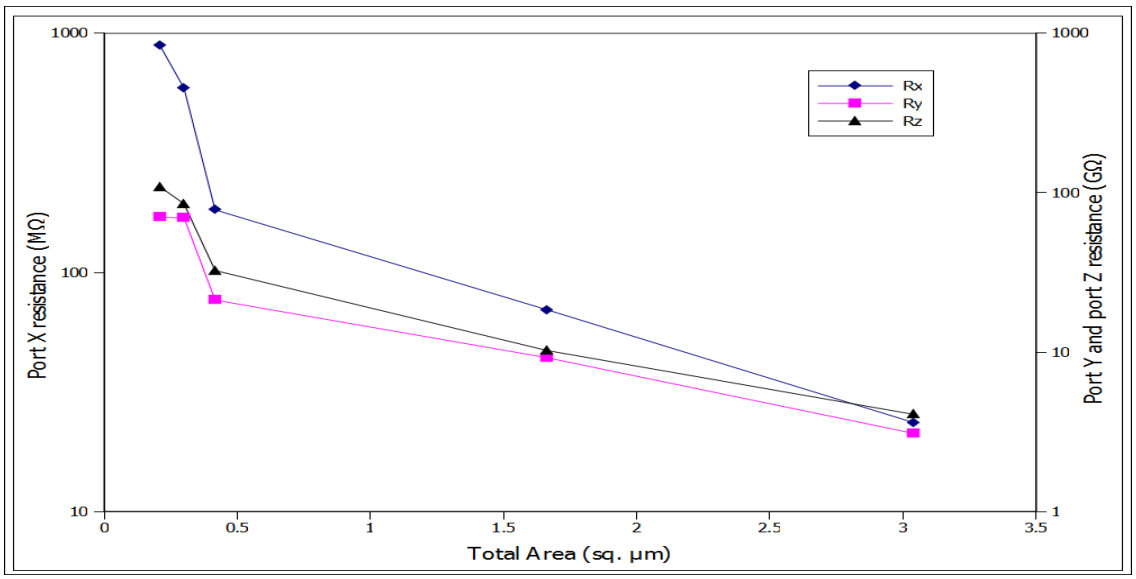

Figure 4.13: Variation of port resistances with total area.

4.5 Variability Analysis of Optimal Design

In order to test the robustness of Design 4 having $L=6L_{min}$, variability analysis is carried out as this has become a metric of equal importance as the challenge is to design reliable circuits with unreliable devices at highly scaled technology node such as 32 nm [97]. Performance parameters (Current gain and voltage gain) of CCII are

estimated with MC (Monte Carlo) simulation using 32 nm PTM [98]. The channel length (L) and channel width (W) are assumed to have independent Gaussian distributions with 3σ variation of 10% [99]. Performance metrics in this work are estimated with 2000 sample size [100].

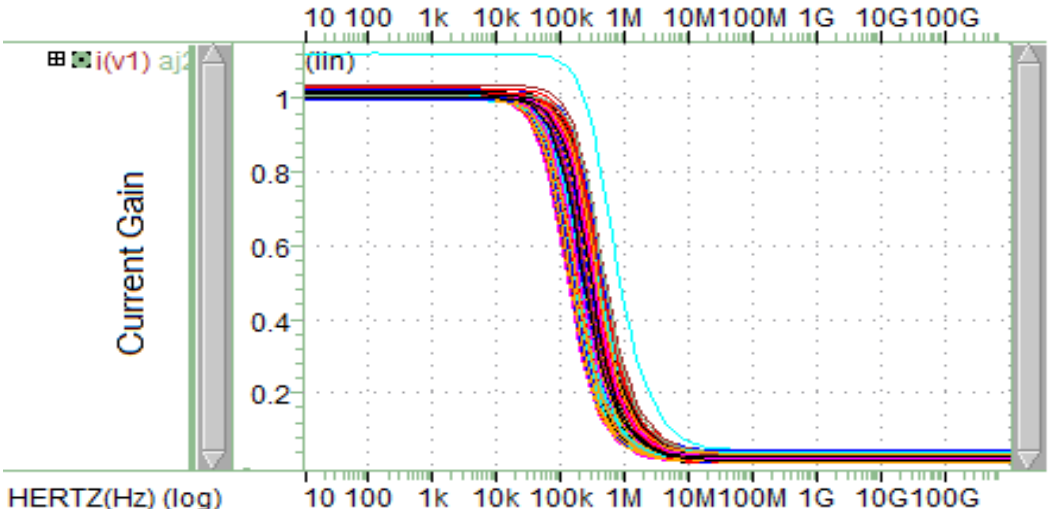

Figure 4.14: Current gain vs Frequency.

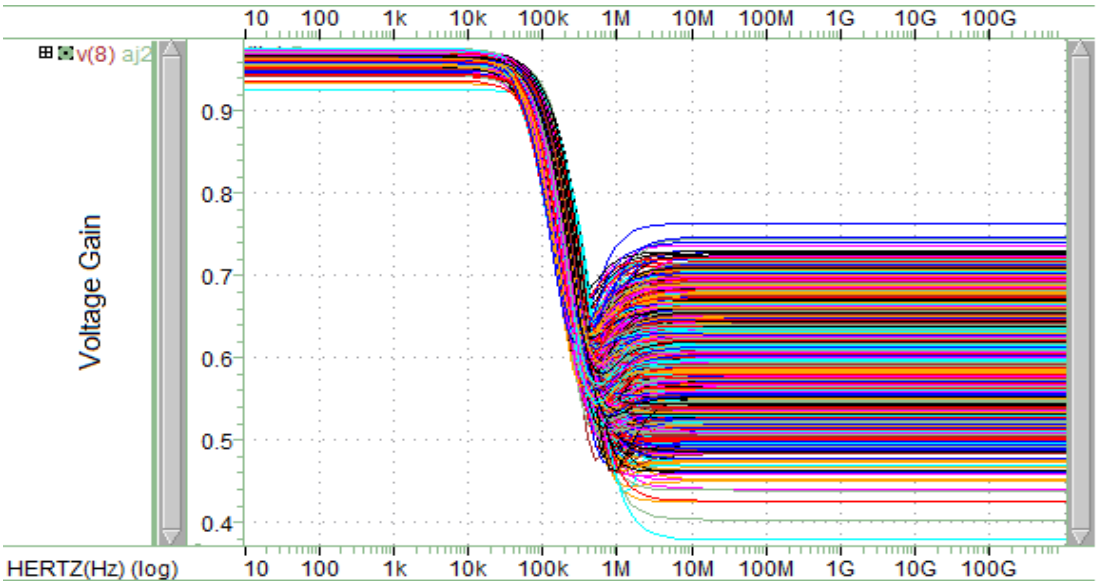

Figure 4.15: Voltage gain vs Frequency.

Figures 4.14-4.15 show Monte Carlo simulation results of the current and voltage gain. It can be observed from these figures that variations in the current and voltage gains are within acceptable limits (closer to unity with ±10% in variation) in the low frequency range where most of the biomedical systems operate.

4.6 Design of Instrumentation Amplifier based on CCII

To validate the optimal design of CCII (Design 4 having $L=6L_{min}$), an instrumentation amplifier, shown in Figure 4.16, is simulated using HSPICE [101]. The amplifier is designed for a differential gain of 27 dB. The frequency response is shown in Figure 17. The simulated gain obtained is 24 dB which shows good agreement with the designed value.

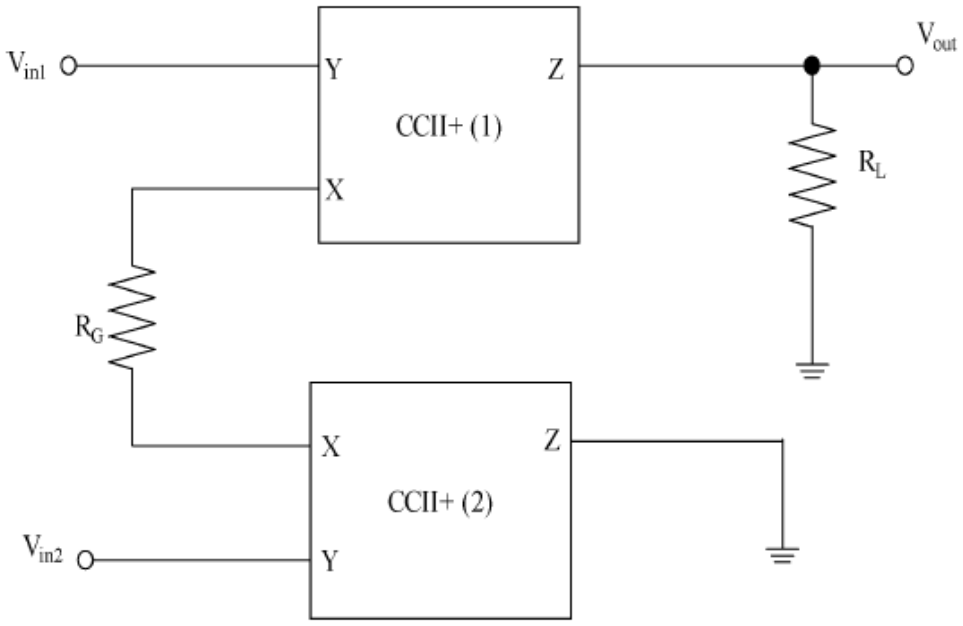

Figure 4.16: Instrumentation Amplifier based on CCII.

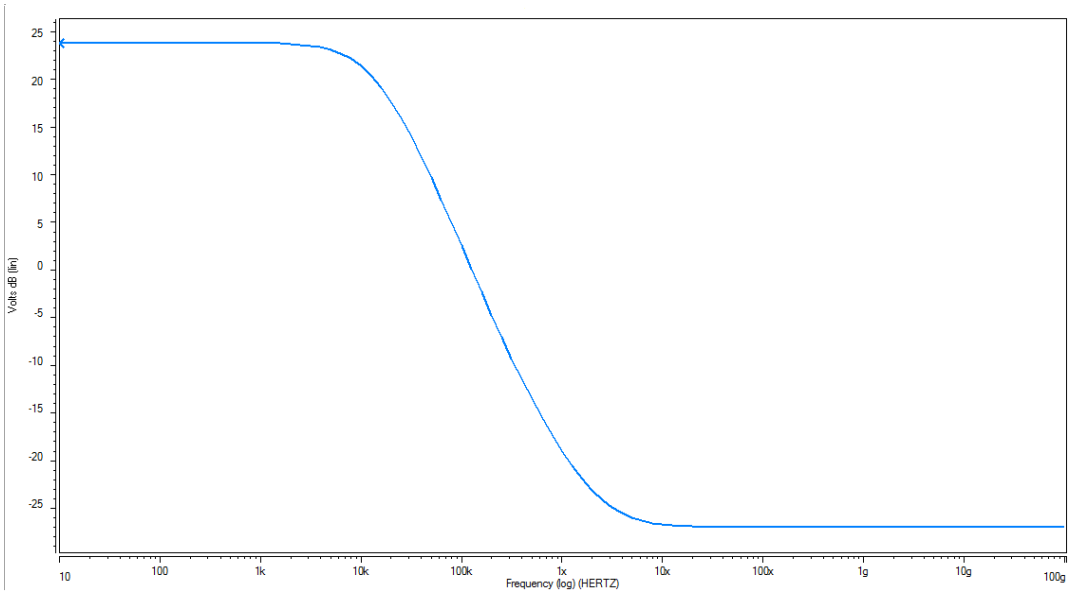

Figure 4.17: Frequency response of Instrumentation Amplifier.

4.7 Summary

This chapter has successfully presented the various designs of second generation current conveyors (CCII) under subthreshold condition. Various performance parameters have been calculated for various designs by choosing the *W/L* ratios in such a way so as to preserve the functionality of the CCII device. The design 4 with $L=6L_{min}$, operating at ±0.25V and at a bias current of 20pA, was found to be optimal and more robust as compared to other designs, thus making it most suitable for ultra low power applications.

The next chapter presents the design and performance evaluation of CMOS and TFET based Second Generation Current conveyor (CCII) at a supply voltage of ±0.3V and bias current of 1nA at 32nm technology node.

CHAPTER 5

Design and Performance Analysis of TFET Based Current Conveyor

Chapter 5

DESIGN AND PERFORMANCE ANALYSIS OF TFET BASED CURRENT CONVEYOR

In current bulk CMOS technology, semiconductor devices are continuously scaled down to achieve higher speed and packing density. This continuous scaling of MOSFET below 45nm technology node gives rise to short channel effects like DIBL, V_t roll off, random dopant fluctuations, mobility degradation etc. There is a need to explore devices beyond bulk CMOS that exhibits higher I_{ON}/I_{OFF} ratio, scalability, better channel electrostatics and robustness against process variations. Tunnel Field Effect Transistor (TFET) is considered as one of the most promising device to provide scaling benefits with significant reduction in short channel effects. This chapter presents a comparative study of CMOS and TFET based Second Generation Current conveyor (CCII) at a supply voltage of ±0.3V and bias current of 1nA at 32nm technology node. The performance parameters of CCII have been investigated in terms of current gain (α), voltage gain (β), current and voltage bandwidths, resistances and their respective bandwidths at various ports of CCII. It has been found that there is considerable improvement in most of the above parameters using TFET.

5.1 Introduction

Complementary metal oxide semiconductor (CMOS) devices are continuously scaled as per Moore's law [10] and the reduction in size has led to a mark improvement in switching speed and packing density. This scaling in advanced CMOS technology results in higher power consumption due to off state leakage and degradation in I_{ON}/I_{OFF} ratio [102]. Current conduction in conventional MOSFETs is based on drift and diffusion mode of transport and the subthreshold swing (SS) is limited by Boltzmann distribution of carriers to as low as 60mV/decade. There is a need to explore new devices that uses other mode of carrier transport at a supply voltage of less than 0.5V together with lower subthreshold swing (<60mV/decade) that maintains high on current with reduced off state current that compete directly with their CMOS counterparts in terms of power, area and speed [4]. The other modes of

carrier transport and device architectures with steeper SS include impact ionization [5, 6], inter-band tunneling transistor [7], ferroelectric FET [8], carbon nanotube transistor [103] etc. Here, the potential of TFET is investigated that can operate well under 0.5V with steeper SS. Moreover, they have reduced temperature sensitivity and variability of its electrical characteristics with the change in conditions [102]. However, devices based on tunneling mechanism failed to meet ITRS standard [9] due to their low ON current. Extensive literature is available on techniques to increase the ON current of tunnel FETs by incorporating double gate and utilizing high-*K* dielectrics like HfO_2 and ZrO_2. To further enhance the ON current, Ge material [47] is employed. The authors in [45] showed that TFETs can be scaled down to nanometric range and still do not suffer from short channel effects like MOS devices and its subthreshold slope is not limited to 60mV/decade. Many authors have reported circuit level performance using TFETs in digital domain but few have come up with its application in the analog world. The authors in [104] proposed a novel 6T Si-TFET based SRAM design for low power applications. In [105], authors have explored the performance of tunnel FET based OTA for ultra low power applications. The 32-bit adder using TFETs is proposed in [106]. Two TFET implementations one utilizing both n and p type TFETs and the other using only nTFETs are presented in [107]. It has critically examined both analog/digital applications of TFETs and has touched upon both device and circuit level performance at 65nm node that emphasized the need of device capacitance optimization together with boosting ON current. The authors in [108] showed that signature characteristics of TFETs such as asymmetry and negative differential resistance (NDR) could be an asset in exploring new topologies for non-linear circuits.

To the best of our knowledge, no one has explored the performance of TFET based current conveyor (CCII) till the writing of this thesis. Hence, this chapter investigates, for the first time, the design and optimization of a tunnel FET based CCII and the results are compared with its CMOS counterpart.

The rest of the chapter is organized as follows: a brief introduction of tunnel FET device is given in section 5.2 followed by an overview of tunnel FET based CCII and its characteristics. In section 5.3, performance parameters of tunnel FET based CCII are presented and are compared with existing bulk CMOS CCII. Section 5.4 deals

with the design of Tunnel FET based instrumentation amplifier and section 5.5 concludes the chapter.

5.2 Tunnel FET device level considerations

5.2.1 Device structure and operation

As discussed in chapter 2, the tunnel FET is a gated p-i-n device structure that is fully compatible with MOS technology. The device structure, shown in Figure 5.1, utilizes double gate structure together with Germanium (Ge) source to boost the ON current. The regions in the tunnel FETs have been named as source, channel and drain respectively in order to be consistent with current MOS technology. The n(p) type device is turned OFF when the gate is held at 0V and turned ON when the positive(negative) voltage is applied to the gate. Source to drain junction is reversed biased in n(p) type device. The current conduction in TFET is through Band to Band Tunneling (BTBT). In n(p) TFET, electrons(holes) tunnel from source valence(conduction) band to drain conduction(valence) band.

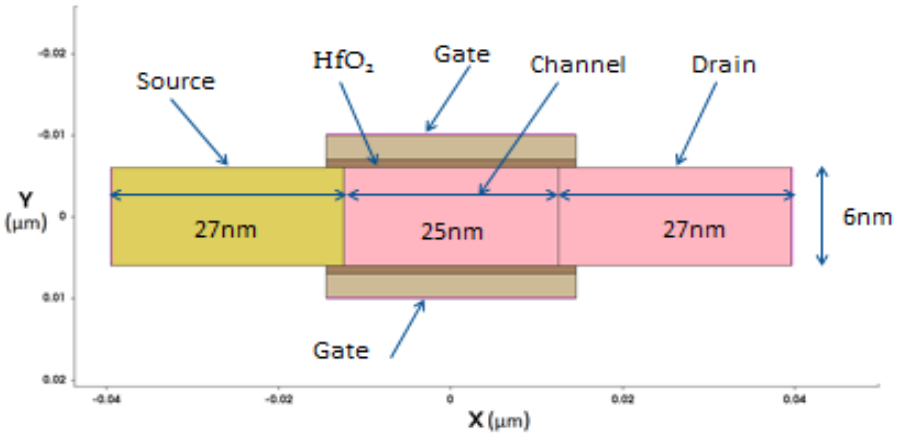

Figure 5.1: Structure of TFET.

5.2.2 Device parameters, modeling and simulation

The tunnel FETs, investigated here, have double gate structures that utilize 'Ge' as source material and are simulated using Synopsys Sentaurus TCAD [109]. Non-local tunneling Kane's model available in Sentauras TCAD [30] is used. Since the source and drain regions are heavily doped and tunneling current is strongly dependent on

band-gap, band-gap narrowing model, oldslotboom is also included. High field saturation mobility model for electrons and holes are also included. Doping in n and p type TFETs is optimized in order to keep high I_{ON}/I_{OFF} ratio. In order to supress the ambipolar effect [110], it is desirable to have high source doping as compared to drain doping. Table 5.1 shows the nominal parameters of the device structure. The doping levels for n(p) type TFET are chosen to be $1x10^{20}$ ($5x10^{20}$), $1x10^{17}$ and $5x10^{18}$ ($5x10^{19}$) atoms/cm^3 for source, intrinsic channel and drain respectively. The work function for gate contact for n(p) type TFET is chosen to be 4.1eV(5.0eV).

The design flow of the modeling of TFET is shown in Figure 5.2. The structure of devices (NFET and TFET) showing grid and doping information is shown in Figures 5.3-5.4. Doping and mesh information together with model parameters act as an input to the Sentaurus device. It is a numeric semiconductor device simulator capable of simulating the electrical, optical and thermal characteristics of various semiconductor devices.

Table 5.1: Nominal Parameters of the Device Structure

Gate Length, L_G	25nm
Oxide thickness, T_{OX}	1nm
Gate dielectric constant	21 ($HfO2$)
Body thickness, T_{Si}	6nm
Gate overlap	2nm
Source/Drain Doping, $N_{S/D}$	$1x10^{20}$ cm^{-3} /$5x10^{18}$ cm^{-3}(N-type) $5x10^{20}$ cm^{-3}/$5x10^{19}$$cm^{-3}$(P-Type)
Channel Doping, N_{Ch}	10^{17} cm^{-3}(P-Type)
Gate work function	4.15eV (N-type), 5.05eV (P-Type)

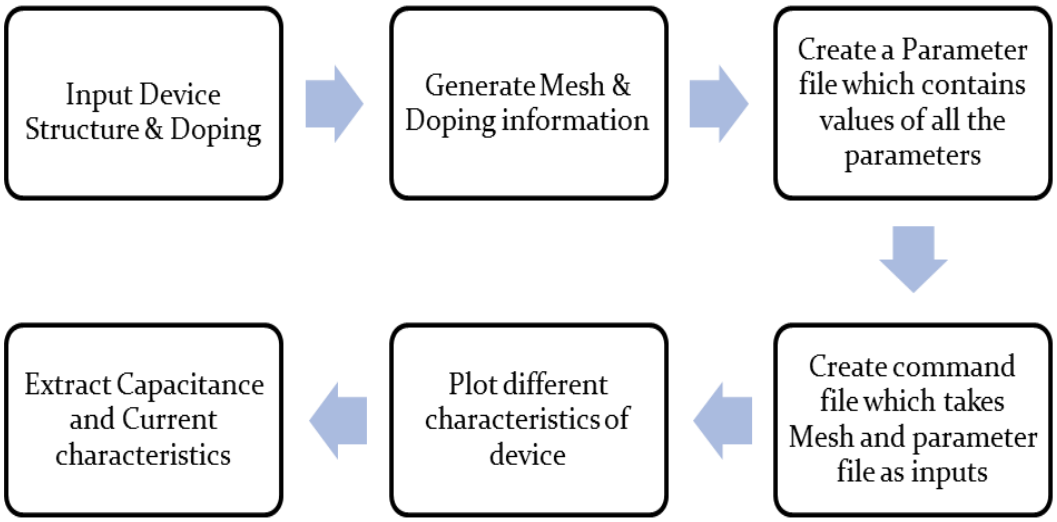

Figure 5.2: Design Flow using Sentaurus Device.

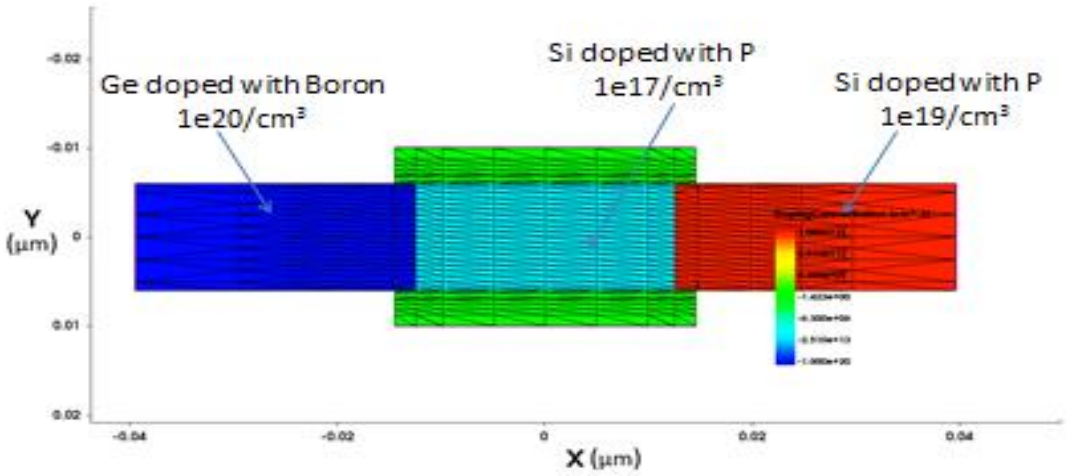

Figure5.3: NTFET Grid and Doping Profile.

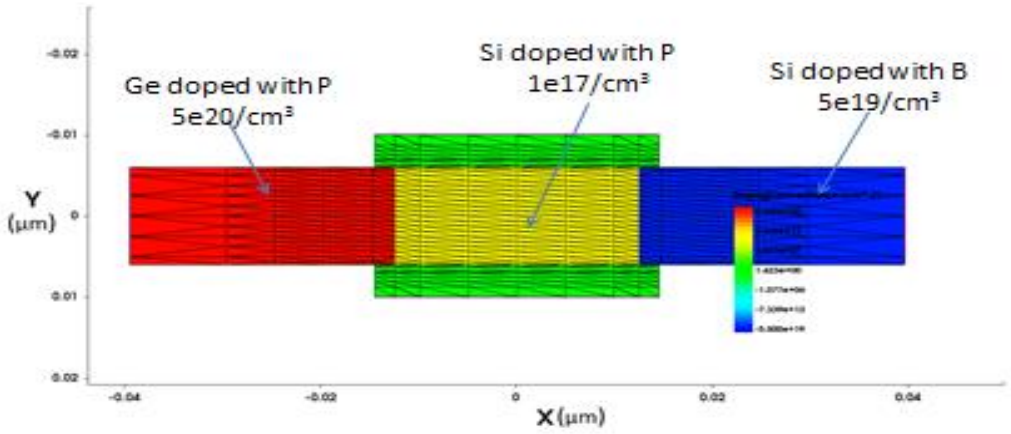

Figure 5.4: PTFET Grid and Doping Profile.

The electrical characteristics and specifications are shown and listed in Figure 5.5 and Table 5.2 respectively.

Table 5.2: TFET Device Electrical Specifications (V_{DD} = 0.4V)

Current specifications	N-type TFET	P-type TFET
I_{ON}(μA/μm)	36	35.63
I_{OFF}(fA/μm)	3.14	0.4

5.2.3 Look-up table based Verilog-A model of TFET

TFET is an emerging device and therefore, no accurate SPICE model is available. Very few analytical models are available in the literature[111, 112] and many are underway. [111] Exhibits lack of the drain control over the channel current. [112] failed to give accurate results at higher gate voltages. This paper, therefore, used a look up table based Verilog-A model obtained from Penn State University, NDCL [113] for the circuit simulation of CCII. The schematic of the Verilog-A transistor model is shown in Figure 5.6. It is a lookup table-based model composed of two-dimensional tables: the transfer characteristics I_{ds} (V_{ds}, V_{gs}), the gate-source capacitance C_{gs} (V_{gs}, V_{ds}) and the gate-drain capacitance C_{gd} (V_{gs}, V_{ds}) across a range of fine-step drain-source voltage bias V_{ds} and gate-source voltage bias V_{gs}. The parasitic series resistance and parasitic external capacitance are not included in the TCAD model, which can be added at the circuit level. Due to the ongoing efforts of p-type Tunnel FET development, we assume almost identical drive-currents for the n-

channel and p-channel transistors in TFET Verilog-A models for the optimal circuit performance. This lookup table based model is very efficient and precise method of modeling upcoming devices whose SPICE models are not available [114]. The Verilog-A module is then used as instances for CCII circuit simulation in HSPICE.

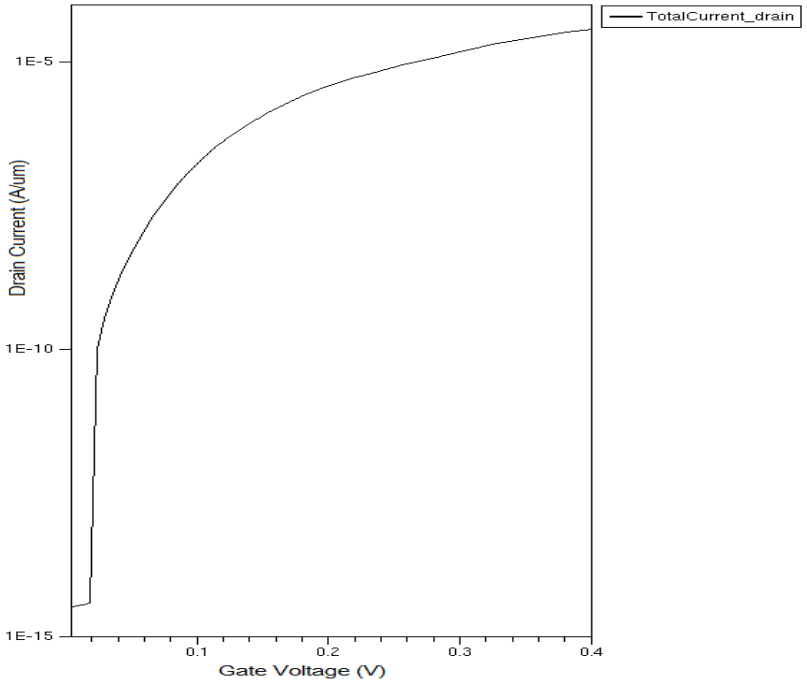

Figure 5.5: Drain Current vs Gate Voltage for NTFET.

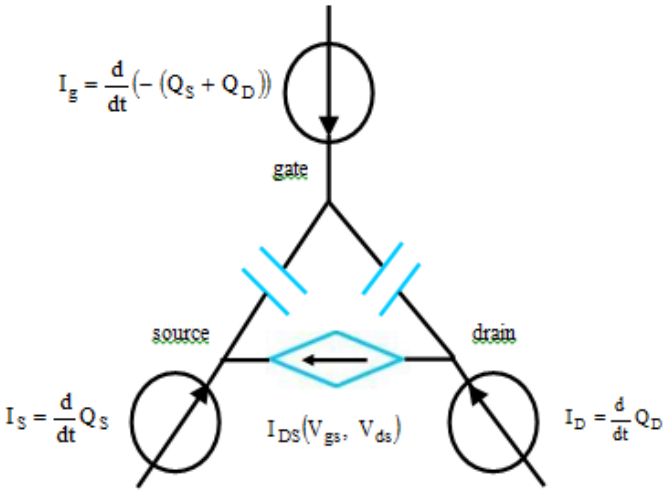

Figure 5.6: Verilog-A model schematic.

5.3 Tunnel FET Based Current Conveyor (CCII)

The functionality and the characteristics of current conveyor (CCII) has been discussed in chapter 4.The diagram representation of TFET based CCII is shown in Figures 5.7.

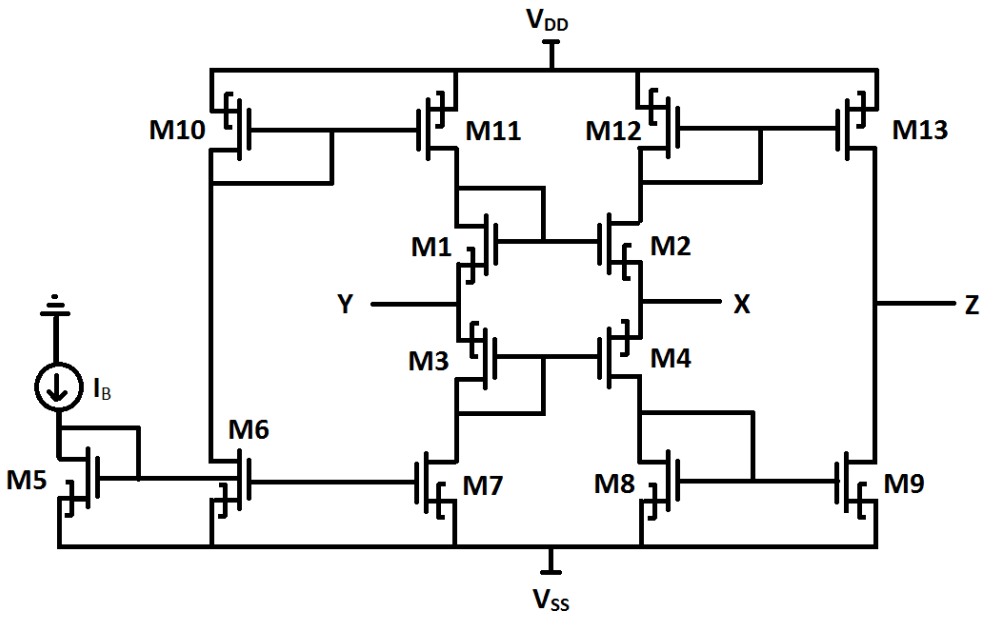

Figure 5.7: Tunnel FET based circuit of CCII.

Various characteristics of TFET-CCII are discussed below and are compared with equivalent MOS-CCII designed in chapter 4 at a voltage of ±0.3V. The aspect ratios of M5-M9 (NMOS) are chosen depending upon silicon area consumption allowance. Depending on the μ_n/μ_p ratio of 32nm technology, aspect ratios of M10-M13 (PMOS) are chosen to be 3.5 times that of M5-M9. For M1-M2 and M3-M4, aspect ratios are chosen to be 1.5 times of M5-M9 and M10-M13 respectively. The lengths of transistors have to be non-minimal in subthreshold design to reduce the current mismatch. Hence, lengths of transistors have been taken five times of L_{min}, which ensures that the current mismatch is within ±10% limit on account of high output resistance. The performance parameters of CCII are listed in Table 5.3. Figure 5.8 and 5.9 show the current and voltage gain variation with respect to the frequency respectively.

Table 5.3: Comparison of CMOS CCII with TFET CCII

	CMOS	**TFET**
V_{DD}	±0.3V	±0.3V
I_B	1nA	1nA
α	1.017	1.113
β	0.9616	0.9613
α 3dB	2.17 MHz	329 MHz
β 3dB	2.73 MHz	Infinite
R_X	19.3 M	2.97 M
R_Y	1.43 G	263.9 M
R_Z	4.10 G	21.3 M
R_X 3dB	4.12MHz	2.04 GHz
R_Y 3dB	17.7 kHz	24.2 MHz
R_Z 3dB	23.7kHz	66.4 MHz

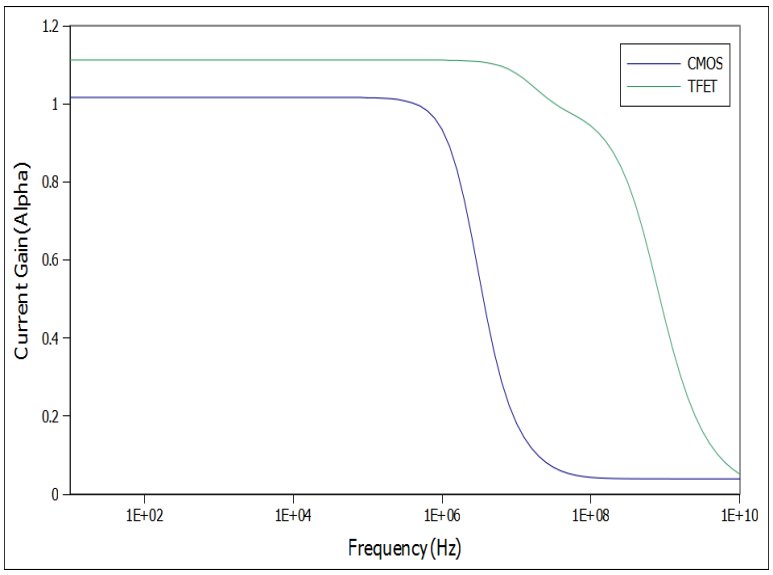

Figure 5.8: Current gain versus Frequency.

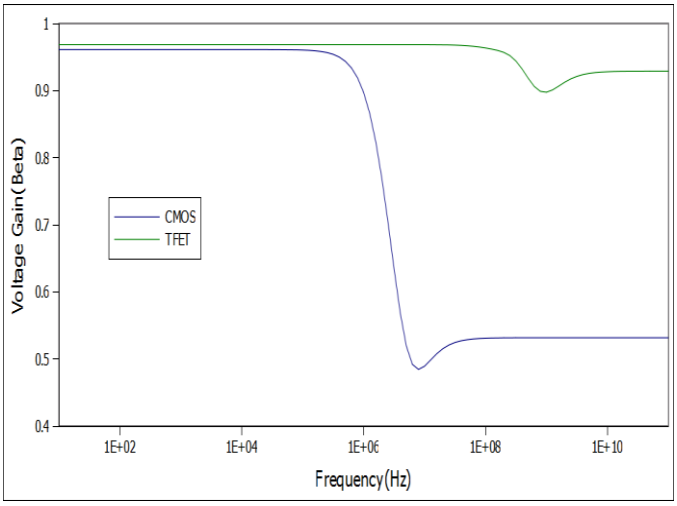

Figure 5.9: Voltage gain versus Frequency.

The current and voltage gains are close to unity that confirms the working principle of current conveyor, but as expected, there is a marked improvement in the 3dB cut off frequency of the tunnel FET based CCII as compared to its MOS based counterpart. TFET devices possess higher g_m/I_d ratio owing to their steeper subthreshold slope (SS) at lower supply voltage. This increase in g_m/I_d results in higher cut off frequency [115]($f_T=g_m/2\pi C_G$), where C_G is the gate capacitance. The next section investigates the performance of an instrumentation amplifier designed by using MOS and TFET based CCII.

5.4 Instrumentation Amplifier

CMOS and TFET CCII based instrumentation amplifier (INA), shown in Figure 5.10, is designed based on [101] and simulated using HSPICE. It is designed for a differential gain of 21dB. The frequency response is shown in Figure 5.11. The simulated gains obtained for the TFET and MOS based INA are 20.5dB and 16.8dB respectively. The higher gain and cut off frequency of TFET based INA is again observed owing to its higher g_m/I_d ratio at lower supply voltage [107]. At extremely low bias current (20pA), the current of the branches M6-M10 and M9-M13 in MOS based CCII doesn't follow proper current mirror action and also due to drain induced barrier lowering (DIBL), MOS based design undergoes excessive leakage and g_m/I_d drops as compared to TFET based CCII**.** Therefore, TFET based INA is more suited for ultra low power operation. However, under large bias condition, MOS based INA is superior than TFET due to the inferior performance of TFET in the superthreshold region.

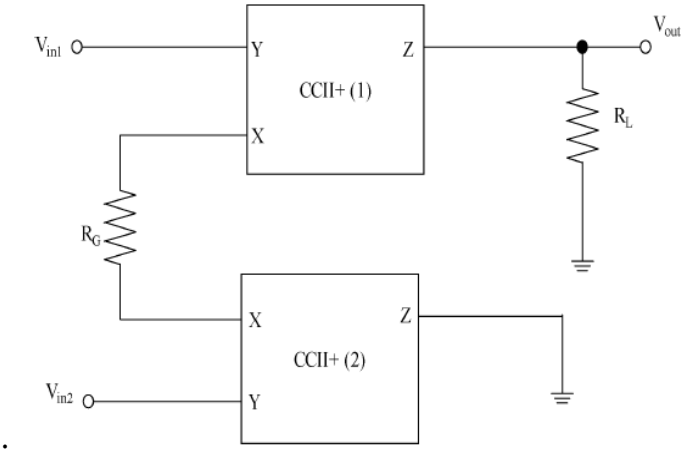

Figure 5.10: Instrumentation Amplifier based on (CMOS/TFET) CCII.

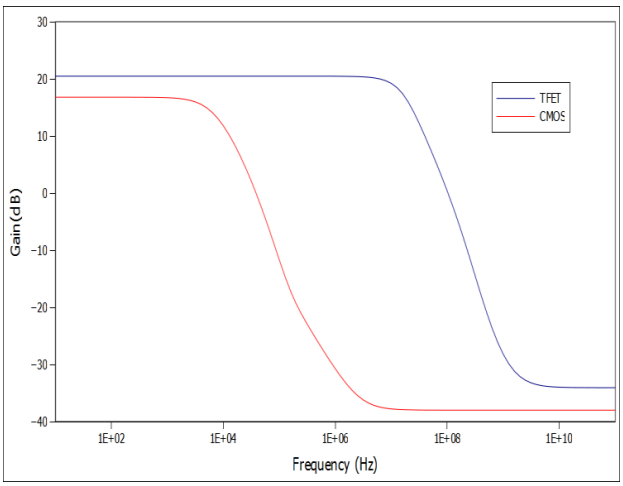

Figure 5.11: Gain (dB) versus Frequency.

5.5 Summary

This chapter has successfully investigated and compared the performance of both TFET and MOS based CCII and instrumentation amplifier at the 32nm technology node. It has been found that TFET based CCII and INA outperformed their MOS based counterparts at low voltage subthreshold operation in terms of gain and bandwidth. The bandwidth power trade-off for MOS devices is limited due to excessive leakage and lower subthreshold slope. Hence, TFET based CCII stands out as an extremely attractive option for ultra low voltage biomedical applications.

The next chapter deals with the design of a CNFET based single ended 6T SRAM cell that saves dynamic as well as static power and maintains higher read stability at the cost of acceptable read/write delay. It proves its robustness by exhibiting narrower spread in various design metrics.

CHAPTER 6

Performance Evaluation of CNFET Based Single-Ended 6T SRAM Cell

Chapter 6

PERFORMANCE EVALUATION OF CNFET BASED SINGLE-ENDED SRAM CELL

Bulk CMOS technology is facing enormous challenges at channel lengths below 45 nm such as gate tunneling, device mismatch, random dopant fluctuations, mobility degradation, etc. Although multiple gate transistors and strained silicon devices overcome some of the bulk CMOS problems, it is sensible to look for revolutionary new materials and devices to replace silicon. It is obvious that future technology materials should exhibit higher mobility, better channel electrostatics, scalability, and robustness against process variations. Carbon nanotube based technology is very promising because it has most of these desired features. There is a need to explore the potential of this emerging technology by designing circuits based on this technology and comparing their performance with that of existing bulk CMOS technology for its rapid commercialization. Due to aggressive scaling, short channel devices are leaky and more prone to process variations compared to long channel MOSFETs. Various leakage components are dominant in short-channel MOSFETs. Therefore, leakage is a serious issue in scaled CMOS technology. This work makes use of CNFET (carbon nanotube field effect transistor) that offers lower leakage, lower variability and better electrostatic control over the channel region. It proposes a CNFET based single-ended 6T SRAM cell that saves dynamic as well as static power and maintains higher read stability at the cost of acceptable read/write delay. It proves its robustness by exhibiting narrower spread in various design metrics.

6.1 Introduction

Due to technology scaling, fluctuations are more pronounced in minimum-geometry devices commonly used in area-constraint circuits such as SRAM cells [116]. SRAM constitutes more than half of chip area and more than half of the number of devices in modern designs [117]. As per ITRS projection, embedded cache will occupy more than 90% of a system on a chip by 2018 [9]. Even today, an H-264 encoder for a high-

definition television requires, at least, a 500 kb memory as a search-window buffer that contributes 40% to its total power consumption [118].

The continuous growth of recent mobile and portable devices/applications has caused a tremendous thrust for low power circuit design. Various methods and techniques, such as SRAM's cell voltage collapsing, increasing virtual ground [119-121], have been applied successfully in the low power/performance region of the design spectrum. Minimum energy operation is possible in subthreshold region. Due to severe increase in V_t fluctuation in subthreshold region caused by global and local process variations in ultra-short-channel devices, 6T SRAM cell and its variants cannot be operated at further scaled supply voltages without parametric and functional failure causing yield loss. The 6T bitcell cannot write in the traditional fashion below 0.6V at 65 nm technology node and beyond [122]. Authors in [123] have developed an RSNM (read-SNM) free 7T SRAM cell, which reduces 30% area overhead compared to read-decoupled 8T SRAM cell (RD-8T) [124, 125]. The RD-8T SRAM cell employs a read buffer which consists of two more transistors than 6T SRAM cell to decouple storage nodes from bitlines. This mitigates the problem of cell stability during read operation. Although this technique made the cell RSNM free, but it could not improve write-ability of the cell. RD-8T cell incurs 20% to 30% area penalty compared to conventional 6T SRAM cell [125]. Addition of two extra transistors to 8T cell in [125] (thus making it 10T cell) enables it to reduce leakage current [122]. RD-8T was developed in [126] by adding peripherals to the original cell. The authors used virtual V_{DD} (supply voltage) scheme to improve write-ability and reduce degradation in write-ability due to PVT (process, voltage, and temperature) variation. Virtual V_{DD} driver, whatsoever small, consumes some leakage power. The authors also added footer circuitry (buffer-foot scheme) to the feet of all the read buffers to pull-up to V_{DD}. This eliminates bitline leakage of unselected cells. However, the buffer-foot scheme requires that the size of the NFET of the buffer to be extremely large, since it has to sink the read current of the entire accessed row. To get around this problem, charge pump circuit was used. Change of cell topology from 6T to 7T and 8T could make the cell RSNM free but could not solve column-interleaving issue for write operation. This issue is addressed by incorporating read-modify-write back scheme [127], which takes extra time for writing during each read operation. Thus, column-interleaving issue is alleviated at the cost of extra read delay. Authors in [128]

reduced leakage power dissipation with use of stack effect in LP10T SRAM cell, but dynamic power such as write power is not considered. PVT variations in design metrics of SRAM cell was reduced by the authors in [129] by use of TG (transmission gate) in place of PG (pass gate) in TG8T SRAM cell. Authors in [130] reduced leakage and impact of process variation in their 11T SRAM cell. Authors in [131] reduced write power and read delay variability in their 13T SRAM cell. These approaches increase the cell area and thus are not suitable for area constrained cache design.

The objective of this chapter is to propose a CNFET based SRAM cell that is scalable to small feature sizes such as 22 nm. The novelty of this cell is that its design requires only six transistors (6T). The architecture of the cell is different from that of conventional 6T SRAM cell which is differential in nature whereas the proposed cell is single ended. The SRAM cells are simulated in HSPICE using the experimentally validated CNFET model [48, 49, 50, and 57] and the 32 nm CMOS Berkeley Predictive Technology Model (BPTM) [132]. The CNFET model has been calibrated to 90% accuracy with experimental data (ac and dc characteristics) from fabricated CNFET circuits [133].

The remainder of the chapter is organized as follows. Section 6.2 presents brief discussion on need for alternative technology for high on/off-state performance and challenges. Threshold voltage for proposed design is estimated in Section 6.3. Section 6.4 presents brief discussion on read/write operation, cell sizing of proposed single-ended 6T SRAM cell. Simulation results are discussed and compared in Section 6.5. Finally, Section 6.6 concludes the chapter.

6.2 Need for alternative technology for high ON/OFF-state performance and its challenges

Moore's law cannot hold forever. Gordon Moore, cofounder of Intel, predicted in 1975, that the number of transistors that could be placed on a chip would double every two years [10]. Reduction of channel length must be realized while preserving so-called long-channel device characteristics (where the vertical gate field rather than horizontal drain field controls the flow of charge carriers). In the past, this has been accomplished by simultaneously scaling the gate length and gate oxide thickness (T_{OX}). However, with T_{OX} approaching 1 nm, gate leakage currents prevent further

reduction. Therefore, ITRS predicts that the end of road on MOSFET scaling will arrive sometime around 2022 with an 11 nm process [9].

As CMOS reaching the scaling limits, the need for alternative technologies are necessary. Nanotechnology-based fabrication is expected to offer the extra density and potential performance to take electronic circuits to the next level. Several nanoscale electronic devices are demonstrated in the recent past by researchers, some of the most promising being carbon nanotube (CNT)-based field effect transistor (CNFET). The CNFETs can be scaled down to 10 nm channel length and 4 nm channel width, thereby enhancing throughput in terms of speed and power compared to the MOSFET. The CNFET circuits with one to ten CNTs per device are about 2-to-10 times faster compared to CMOS circuits [134]. Today's CNFETs reach transconductance values (g_m) per tube in the 10-20 μS range [135, 136] with the theoretically predicted values as high as ~ 60 μS [137].

CNTs can be either semiconducting or metallic; semiconducting CNTs (s-CNTs) are useful for CNFET, whereas metallic CNTs (m-CNTs) in the channel cause shorts between the source and the drain causing excess leakage/malfunctioning of logic circuit. The shortcoming of the CNFET-based design is that there are some fabrication issues, which are likely to be overcome shortly. CNFET-based circuit with small width CNFET suffers from CNT-specific imperfections such as 1) CNT diameter variations, 2) CNT density (count) variations, 3) Mis-positioned CNTs and 4) presence of m-CNTs. All of the above imperfections can directly cause variations in the drive currents of CNFETs, which lead to circuit performance variations. These imperfections can even result in complete failure of CNFET-based circuits when there are no s-CNTs between the source and drain [138]. All the above CNT-specific imperfections exhibit an inverse dependence of I_{ON} (ON current) variability on square root of CNT count ($\sigma_{Ion}/\mu_{Ion} \alpha 1/\sqrt{N}$). This effect is commonly known as statistical averaging [139]. Therefore, variations and failure probability caused by CNT-specific imperfections can be reduced to an acceptable level by utilizing wide CNFETs that contain many CNTs. Of course, this approach of upsizing CNFETs for variability improvement is very expensive at highly scaled technology nodes. Large degree of spatial correlation is observed in directional CNT growth. Maximum benefits from such correlation can be realized by enforcing the active regions of CNFETs to be aligned with each other. The full benefits of CNT correlation is realized by enforcing

layout restrictions in the active regions. This relaxes the device-level failure probability by 350× at the 45 nm technology node, leading to significantly reduced costs associated with upsizing CNFETs [138].

For a growth process that yields uniformly distributed chiralities, one-third of CNTs will be metallic (since one-third of all possible chiralities yield metallic CNTs). Typical CNT synthesis techniques yield ~33% metallic CNTs [141]. In another typical experiment, authors in [142] found 25%–50% m-CNTs. All known CNT growth techniques are prone to inherent CNT imperfections due to metallic and mis-positioned CNTs. These imperfections result in unacceptably high leakage currents, severely increased susceptibility to noise, unpredictable circuit delays, and incorrect digital logic functionality. However, preferential s-CNT growth technique yields 90%-96% s-CNTs [143, 144]. Reduction of m-CNTs has also been demonstrated when CNTs are deposited onto the wafer via a self-sorting m-CNT reduction technique that yields 1%-10% m-CNT [145, 146]. For VLSI CNFET circuits, the percentage of m-CNTs must be reduced to less than 0.01% [147]. Metallic CNTs can also be removed after growth by selective chemical etching [148] or current-induced breakdown [149]. In current-induced breakdown technique, s-CNTs are switched off using gate voltage and a large voltage V_{DS} (drain-to-source voltage) is applied across the source and drain of the CNFET. Large currents flowing through the m-CNTs induce self-heating of m-CNTs, causing them to break down by oxidation [149, 150]. VMR (**V**LSI-Compatible metallic CNT **r**emoval) technique also overcomes challenges posed by m-CNTs. In this technique, a special layout called VMR structure is fabricated. Next, VLSI-compatible m-CNT electrical breakdown is performed by applying high voltage across m-CNTs using the VMR structure. In this process, the Si-substrate acts as back-gate that turns off s-CNTs. After m-CNT breakdown, all VMR structures exhibit high I_{ON} to I_{OFF} ratio [151]. Authors in [152] experimentally demonstrated an automated technique for generating misaligned and mis-positioned CNT-immune logic circuit designs that are guaranteed to implement correct functions even in the presence of a large number of misaligned and mis-positioned CNTs.

The performance of CNFET has been significantly improved since the first fabricated device in 1998. It is evident from the above discussion that most of the CNT-specific fabrication issues have been solved. Moreover, CNFET can be fabricated using the existing Si-CMOS infrastructure and it can also be integrated with Si-CMOS on the

same chip [140]. It means that most of the fabrication issues have been solved and CNFET technology holds a lot of promise. At the end, it is also important to investigate the potential of systems designed in this upcoming technology for their rapid commercialization once the technology matures. This chapter is an effort in that direction.

6.3 Estimation of Threshold Voltage for the Proposed Design

CNT is categorized as SWCNT (single-walled carbon nanotube) and MWCNT (multi-walled carbon nanotube). Most SWCNTs have a diameter close to 1 nm with a tube length that can be many millions of times longer. The structure of a SWCNT can be conceptualized by wrapping a one-atom-thick layer of graphite called graphene into a flawless cylinder. SWCNT based CNFETs are used in this design. The property of SWCNT depends on its chirality (n_1, n_2) − the direction in which it is rolled up. The CNT acts as semiconductor if $n_1 \neq n_2$ or $(n_1 - n_2)/3 \neq i$, where i is an integer. Otherwise, CNT works as a metal. The D_{CNT} (diameter of CNT) is estimated using its chirality vector (n_1, n_2) as [48, 49, 50, and 57]

$$D_{CNT} = \frac{a}{\pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{6.1}$$

The V_t (threshold voltage) of a CNFET can be approximated to the first order as the half bandgap, which is an inverse function of D_{CNT} [153]

$$V_t \approx \frac{E_g}{2q} = \frac{1}{\sqrt{3}}\frac{aV_\pi}{qD_{CNT}} \tag{6.2}$$

where E_g is energy gap, q = electronic charge, $a = \sqrt{3}d = 2.49$ Å is the lattice constant (where $d \approx 1.44$ Å is the inter-carbon-atom distance) and $V_\pi = 3.033$ eV is the carbon π–to–π bond energy in the tight bonding model. The use of appropriate D_{CNT} and hence V_t of CNFETs is a critical piece of our design strategy. In this work, multi-V_t and multi-diameter CNFETs are used with chiral vector values (11, 0), (14, 0) and (19, 0). The D_{CNT} of the CNFET with chiral vector values (11, 0), (14, 0) and (19, 0) are estimated using (6.1) to be 0.8719 nm, 1.1088 nm and 1.5 nm respectively. The V_t of the CNFET with chiral vector value of (11, 0), (14, 0) and (19, 0) are estimated using (6.2) to be 0.5018 V, 0.394 V and 0.29 V respectively. Other important CNFET

technology parameters are tabulated in Table 6.1(a). The chirality vector, V_t and D_{CNT} of employed CNFET in proposed design are presented Table 6.1(b).

Table 6.1 (a) Device and Technology Parameters of CNFET used in the Proposed Design (SE-6T)

(b) Device Parameters of Proposed Design

(a)

Parameter	Description	Value
L_{ch}	Physical channel length	22 nm
W_g	Width of metal gate (sub_pitch)	6.4 nm
T_{OX}	Thickness of high-k top gate dielectric material	4 nm
Kox	Dielectric constant of high-k top gate oxide material	16
(n_1, n_2)	Chirality of CNT used in CNFET	(11,0),(14,0),(19,0)
n_CNT	Number of tube per device	5

(b)

CNFETs	Chirality vector (n1, n2)	Threshold Voltage (V)	Diameter (nm)
MP1	(11, 0)	−0.5018	0.8719
MP2	(11, 0)	-0.5018	0.8719
MN1	(19, 0)	0.29	1.5
MN2	(14, 0)	0.394	1.1088
MN3	(19, 0)	0.29	1.5
MN5	(19, 0)	0.29	1.5
MN4	(19, 0)	0.29	1.5

6.4 Read/Write Operation and Cell Sizing of Proposed Design

Figure 6.1 (a) and (b) show schematics of differential 6T SRAM cell (Dif-6T) and the proposed single ended 6T SRAM cell respectively. Figure 6.2 shows cell layout of proposed CNFET-based single-ended cell.

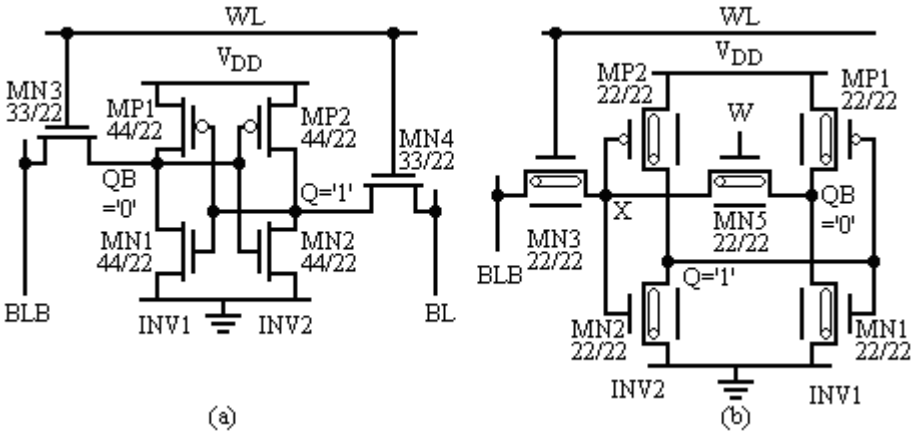

Figure 6.1: (a) Differential 6T SRAM cell (Dif-6T), (b) Proposed CNFET-based single ended 6T SRAM cell (SE-6T).

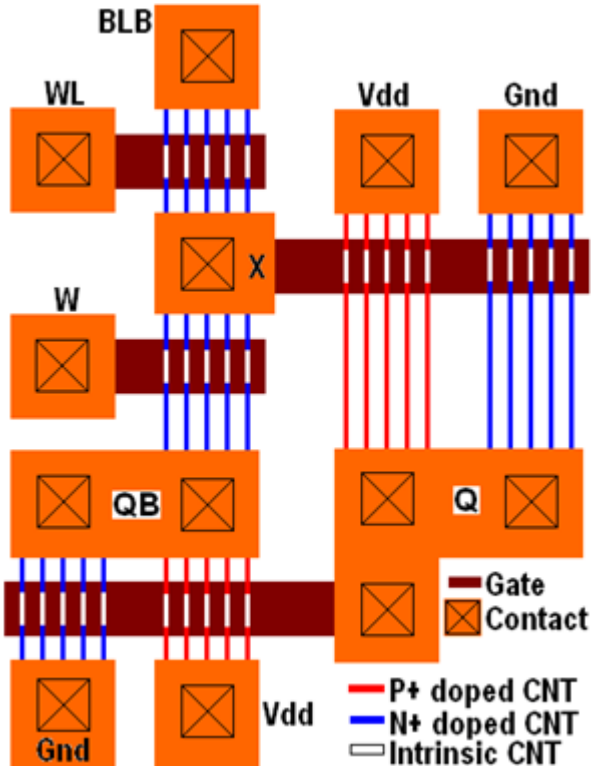

Figure 6.2. Cell layout of proposed CNFET-based single-ended cell.

Before and after each write operation BLB is pre-charged. Write operation of SE-6T is initiated by switching MN5 off by applying W = "0". This breaks the feedback path and makes writing easier. In the literature, single ended 5T SRAM cell is found, which exhibits problem while writing "1" and needs write assist method [154]. This work mitigates this problem to a large extent. BLB carries the complement of the bit to be stored in storage node Q. When WL (wordline) is asserted high, bit applied to

BLB gets complemented and stored in storage node Q. This bit in turn drives INV1 (inverter 1) and finally a bit applied to BLB gets stored in QB. Thus, write operation involves two inverter delay and hence requires longer write time than Dif-6T. As MN3 passes a bad "1" at the end of write "1" operation to QB, V_X is at lower voltage than V_{QB}. Just after write operation, in hold mode, W is raised high and X is raised gradually. During this transition time, MP2 may be partially on causing short circuit current to pass through MN2 to ground.

This problem can be mitigated in two ways: 1) by using high$-V_t$ MP2 (absolute value), thereby making INV2 (inverter 2) a LO-skewed inverter which ensures that V_M (switching threshold) of INV2 is less than $V_{DD}/2$; and 2) using low V_t MN5 to reduce voltage difference between QB and X (if $\beta_p/\beta_n < 1$, the inverter is LO-skewed and its $V_M < V_{DD}/2$, where $\beta = \mu C_{ox}(W/L)$). In this chapter, both techniques are used. The INV2 is made LO-skewed by using high-V_t MP2 (absolute value). The V_t used for MP2 is −0.5018 V and V_t used for MN5 is 0.29 V. Extensive simulations are carried out to obtain optimum results by selecting different diameters (and hence V_ts). Optimum results in terms of various design metrics are obtained with the selection of parameters tabulated in Table 6.1(b).

Before read operation, BLB is pre-charged to V_{DD}. Then WL is asserted high and MN5 is switched on applying "1" to W (rather it remains ON during hold mode). BLB drops through the critical read path MN3, MN5 and MN1 with QB storing "0". A single-ended sensor or an inverter detects this voltage drop in BLB. While reading with QB storing "1", BLB is not discharged and is directly sensed from the pre-charged BLB.

6.5 Simulation Results and Discussions

This section presents comparison of various design metrics which are estimated during Monte Carlo simulation using 22 nm PTM. The channel length (L), channel doping concentration ($NDEP$), oxide thickness (T_{OX}), threshold voltage (V_t), width of metal gate (W_g), and pitch are assumed to have independent Gaussian distributions with 3σ variation of 10%.

6.5.1 Standby Power

Standby leakage in embedded cache is an alarming issue in deep submicron technology. The leakage current is one of the major contributors to the total power dissipation in SRAM cell as whole part of the cache remains idle most of the time except the row being accessed. It consumes 2.25× lower standby power. It proves its robustness against process variations by featuring 2.15× narrower spread in standby power distribution. This improvement is achieved due to employed CNFET that is more robust against process variations compared to CMOS. This is due to its cylindrical geometry, a variation in the gate oxide thickness that strongly affects the drive current and capacitance of CMOS transistors has a negligible impact on the CNFET's operation. This is evident from Figure 6.3, which shows the N-MOSFET and N-CNFET leakage characteristics as supply voltage is scaled down. An N-MOSFET exhibits 13.85× higher leakage at 25°C at nominal supply voltage of 0.8 V compared to an N-CNFET.

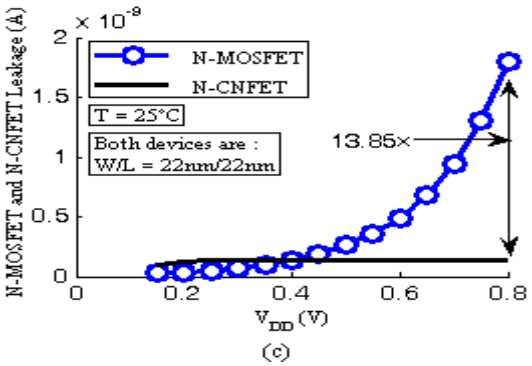

Figure 6.3: N-MOSFET and N-CNFET leakage versus V_{DD}.

6.5.2 Read Stability and Write Ability

The static noise margin (SNM i.e., hold SNM) of SRAM cell is defined as the minimum DC noise voltage necessary to flip the state of the cell. SNM of an SRAM is a widely used design metric that measures the cell stability. Figure 6.4(a) and Figure 6.4(b) show conceptual test setups for measuring SNM of SE-6T and Dif-6T respectively. However, the SRAM cell is most vulnerable to noise during read access since the "0" storing node rises to a voltage higher than ground due to a voltage division along the access transistors (MN3/4) and inverter pull-down NMOS devices

(MN1/2). The ratio of the widths of the pull-down transistor to the access transistor, commonly referred to as the cell ratio or β ratio, determines how high the "0" storage node rises during a read access. Therefore, RSNM (read static noise margin) is a more critical design metric of SRAM cell than SNM (hold SNM). RSNM of both designs are estimated using butterfly curve. The conceptual test setups for measurement of RSNM of SE-6T and Dif-6T are shown in Figure 6.5(a) and Figure 6.5(b) respectively. The butterfly curves for RSNM are shown in Figure 6.6 (a). As observed from Figure 6.6(a), the SE-6T outperforms Dif-6T in terms of 2.38× improvement in RSNM. This improvement in RSNM is achieved due to the low-V_t pull-down transistors (MN1 and MN2) and high-V_t access transistor (MN3) in SE-6T. This implies that switching thresholds of both inverters are lower than that of Dif-6T. This has shifted the VTC (voltage transfer curve) of INV1 (inverter 1) to the left and pushed VTC^{-1} (inverse VTC) of INV2 (inverter 2) down making both the lobes of the butterfly curve wider. However, the lobes are unequal due to asymmetric read paths. As mentioned above, SE-6T offers much higher read stability at the cost of lower write ability as shown in Figure 6.6 (b). Our simulation results shown in Figure 6.6 (a) and (b) are found to be in good agreement with the general trend published in the literature, since it is an established fact that the read stability and write-ability are the two conflicting design metrics of an SRAM cell.

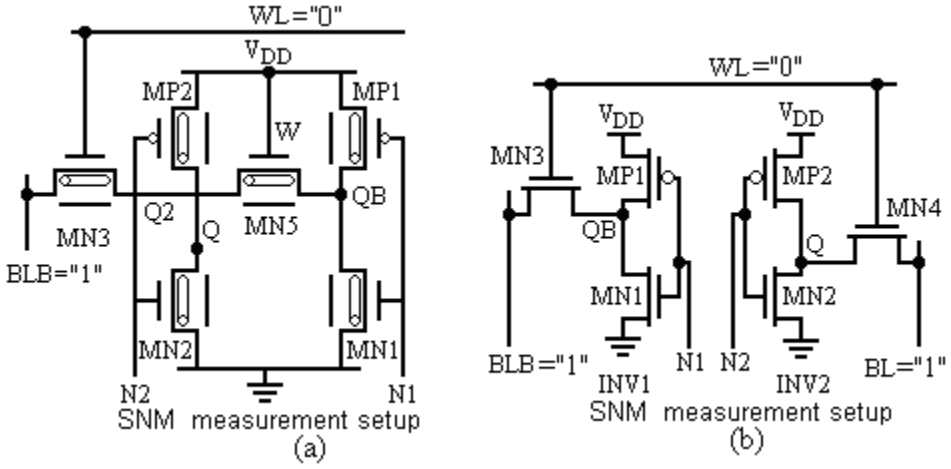

Figure 6.4: Test circuit for measurement of SNM of (a) SE-6T, and (b) Dif-6T.

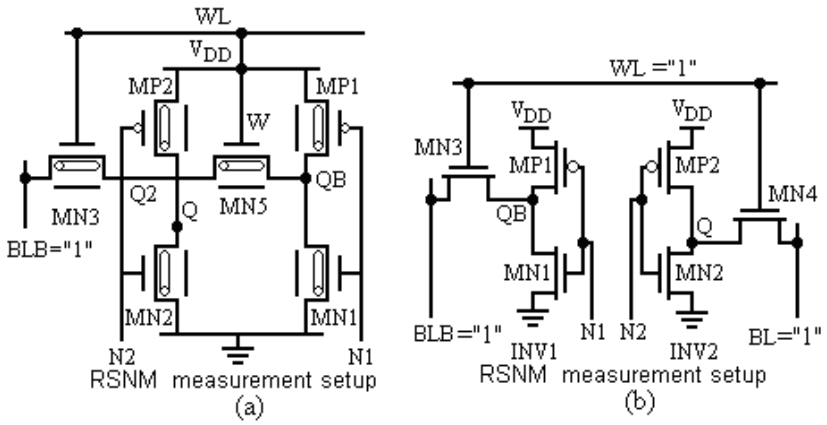

Figure 6.5: Test circuit for measurement of RSNM of (a) SE-6T, and (b) Dif-6T.

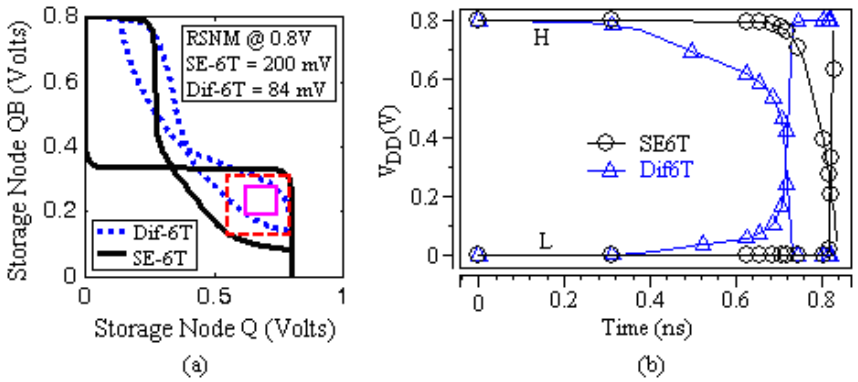

Figure 6.6: (a) Static voltage characteristics of SRAM cells during read operation, (b) Write-ability.

6.5.3 Read Delay and its Variability

The worst case read delay occurs while reading QB storing "0". This is because the read path is longer in case of SE-6T compared to Dif-6T in this particular read operation. The proposed design incurs 1.25× longer read delay in this worst-case condition in spite of low-V_t transistors used in this critical read path as shown in Figure 6.7 (a). Another likely cause is attributed to the fact that the read operation is completed when BLB drops more than 50% (read delay is estimated from the time when WL is activated till BLB drops by 55% in case of SE-6T and 10% in case of Dif-6T) to ensure misread since proposed design is single-ended. The proposed design shows its robustness by offering 1.67× narrower spread in read delay. This improvement is achieved due to longer read path since longer logic depth exhibits less variability.

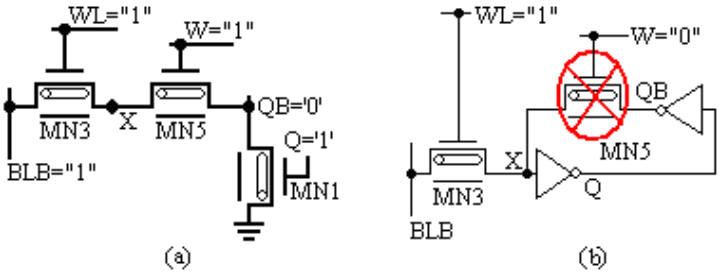

Figure 6.7: (a) Worst-case read delay due to critical read path and (b) Longer write delay due to two inverters' delay for storing a bit in L.

6.5.4 Write Delay and its Variability

The T_{WA} is estimated as the time required for writing "0" to storage node QB from the point when WL reaches 50% of its full swing (from its initial ground level) to the point when QB falls to 10% from its initial high value (i.e., its 90% swing). Similarly, T_{WA} for writing "1" to QB is estimated from the point when WL reaches 50% of its full swing (from its initial ground level) to the point when QB rises to 90% from its initial low level. As discussed in Section 6.4, for writing a bit to QB, the write operation is completed after a two inverter delays when QB settles to its new state. Therefore, the T_{WA} is longer than T_{RA} as shown in Section 6.5. Writing a bit to QB write operation is completed after two inverter delays when QB settles to its new state as shown in Figure 6.7 (b). Therefore, the write delay of SE-6T is longer than that of Dif-6T. The SE-6T shows 1.15× longer write delay compared to Dif-6T. As per our simulation results, the proposed design shows 1.12× narrower spread in write delay proving its robustness.

6.6 Summary

This chapter successfully presents a CNFET based single ended 6T SRAM cell which is capable of saving dynamic and static power. The simulation results confirm its successful functionality, read stability and improved immunity against PVT variations. The benefits of static power reduction along with improvement in RSNM make it an attractive choice for applications (such as L3 cache) where read/write delay is of less concern.

The next chapter presents a reconfigurable, low power four quadrant memristor and carbon nanotube field effect Transistor (CNFET) based analog multiplier. The proposed multiplier is operated at low supply voltage providing extremely large bandwidth and consuming very little power.

CHAPTER 7

Reconfigurable Memristor and CNFET Based Four Quadrant Multiplier

Chapter 7

RECONFIGURABLE MEMRISTOR AND CNFET BASED FOUR QUADRANT MULTIPLIER

In this chapter, a reconfigurable, low power four quadrant memristor and carbon nanotube field effect Transistor (CNFET) based analog multiplier is proposed. The proposed multiplier is verified by extensive HSPICE simulations using experimentally verified memristor and Stanford CNFET models that have been calibrated for 90% accuracy at the 32nm technology node. The proposed multiplier has an input range of ±0.25V, extremely large bandwidth of 30.5 GHz, and consumes just 43.8μW of power along with low total harmonic distortion (THD% ≤0.75) and significant noise suppression at a supply voltage of ±0.3V.

7.1 Introduction

Analog multiplier is an important building block of analog signal processing systems. It is used as a sub-circuit for many applications such as adaptive filters, modulators, phase comparators, frequency mixers, and neural networks [155]. It performs linear product of two analog input signals x and y, yielding an output z=*K*xy, where '*K'* is a constant of proportionality [156]. The basic principle involved in the design of a multiplier is a quarter square algebraic identity [157]. There are three operations which need to be performed. The first operation to be performed is the summation and difference of the input signals. The second step is the squaring of the obtained sum and difference. In the last step, the output is taken as the difference between the obtained squared signals. Motivated by the work of Gilbert [158], multipliers have been designed and optimized for a variety of applications [159-162]. The basic idea behind these designs is the utilization of active devices like CMOS to process/condition the input signals followed by the neutralization/minimization of errors due to the non-linear characteristics of these devices. Active devices are continuously scaled to achieve high packing density, high speed and low power

consumption. Due to leakage current, high field effect, short channel effect and lithographic issues associated with CMOS, Moore's law[10] cannot hold for ever and there is a need to explore emerging devices like CNFET that has the potential to replace existing bulk CMOS along with a memristor to sustain Moore's law far in the future. This chapter proposes a memristor and CNFET based multiplier that operates at low voltage with high linearity, large input signal swing and better frequency response.

The remainder of this chapter is organized in the following sections. Memristor is introduced in section 7.2. The proposed multiplier is illustrated in section 7.3. The simulated results of the proposed multiplier are then presented in Section 7.4 followed by summary of the chapter in section 7.5.

7.2 Emerging Devices

7.2.1 Memristor

Memristor was hypothesized by Leon Chua in 1971 [163]. The idea was based on a simple symmetry argument that a fourth fundamental 2-terminal passive circuit element is necessary to complement the other three. The memristor is like a potentiometer which permits continuous change in its resistance. It differs from potentiometer in the sense that a memristor has only two terminals and the resistance is changed by applying different writing and erasing potentials across the device. It can remember its previous state when power is removed, and hence the device has memory.

The physical device consists of a thin layer of TiO_2 (Titanium dioxide) sandwiched between two metal contacts made of Pt (Platinum) as shown in Figure 7.1. The oxide film is divided into two regions: a doped region of TiO_{2-x} with low resistance R_{ON} due to the high concentration of dopants and an undoped region of TiO_2 with high resistance R_{OFF}. The ratio between the two is controlled by the position of the boundary between the doped and undoped regions. As the device has extremely small dimensions, a very strong electric field develops when a voltage is applied. This causes the oxygen vacancies to move towards or away from the doped region effectively changing the position of the boundary between the two regions and hence the total resistance of the device [164].

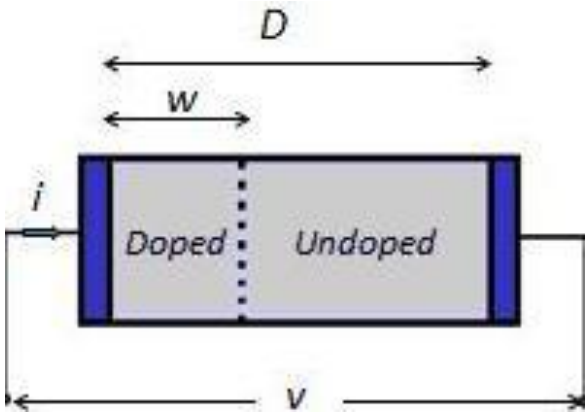

Figure 7.1: Basic Structure of Memristor.

The total resistance of the memristor, R_{mem}, can be modelled as the sum of the resistances of the doped and undoped regions.

$$R_{mem}(x) = R_{ON}x + R_{OFF}(1-x) \tag{7.1}$$

$$x = \frac{w}{D} \in (0,1) \tag{7.2}$$

R_{ON} is the resistance of completely doped memristor and R_{OFF} is the resistance of completely undoped memristor corresponding to $w=D$ and $w=0$ respectively where 'w' is the width of the doped region and 'D' is the total width of the memristor.

The relation between excitation voltage and current flowing through the memristor is

$$v(t) = R_{mem}(w)i(t) \tag{7.3}$$

The dependence between the passing current 'i' and the x state is governed by the dynamic state equation [165]

$$\frac{dx}{dt} = kf(x)i(t), \qquad k = \frac{\mu_v R_{ON}}{D^2} \tag{7.4}$$

Where μ_v is the average dopant mobility. The function f(x) in equation 7.4 is a window function and models the non-linearity of the charge carrier transport in the memristor. It is given by [166]

$$f(x) = 1-(2x-1)^{2p} \tag{7.5}$$

where 'p' is an integer.

Apart from having nanoscale dimensions, memristor has other useful properties as well like reconfigurability, continuous resistance range, low-power consumption etc. There are many applications of memristors. Analog programmable circuits have already been explored theoretically, mostly through simulations. Some of the examples are: Analog filters, gain amplifiers, threshold comparators, switching thresholds Schmitt triggers and frequency relaxation oscillators [167-170]. In all these examples, characteristics of the circuit were configured by adjusting the resistance of the memristor.

7.2.2 Carbon Nanotubes FET (CNFET)

This emerging device has been discussed thoroughly in chapters 2 and 6. There it has been shown that the working principle of CNFET is similar to that of conventional MOSFET. The bulk semiconductor channel is replaced by a number of semiconducting carbon nanotubes. Since the carriers are now confined to a narrow nanotube, their mobility increases due to quasi 1-D (ballistic) transport. This chapter deals exclusively with SWCNTs only and the multiplier circuit is operated in the voltage range from ±0.2V to ±0.9V, therefore it has been implemented using SWCNTs due to higher drive current and transconductance, lower on resistance and negligible off current as compared to MOSFET.

7.3 Proposed Multiplier

The idea behind the design of proposed multiplier is the quarter square algebraic identity [157]. The proposed multiplier circuit is shown in Figure 7.2. It consists of two stages. The first stage is the adder subtractor stage consisting of memristive voltage dividers and the second stage is the multiplier core where input voltage is first converted to current and finally current is converted to voltage and differential output is taken. The differential output can be expressed as:

$$V_{out} = \left[(V1+V2)^2 - (V1-V2)^2\right] = 4V1V2 \qquad 7.6$$

The most prominent feature of the proposed multiplier is its reconfigurability due to memristive voltage divider. Apart from that its area can be estimated to be smaller than other multipliers because of the nanoscale memristive devices. Also the memristive voltage divider functions as an adder and a subtractor for a large range of

frequencies. All these features make this multiplier suitable for portable systems where power consumption is an important factor.

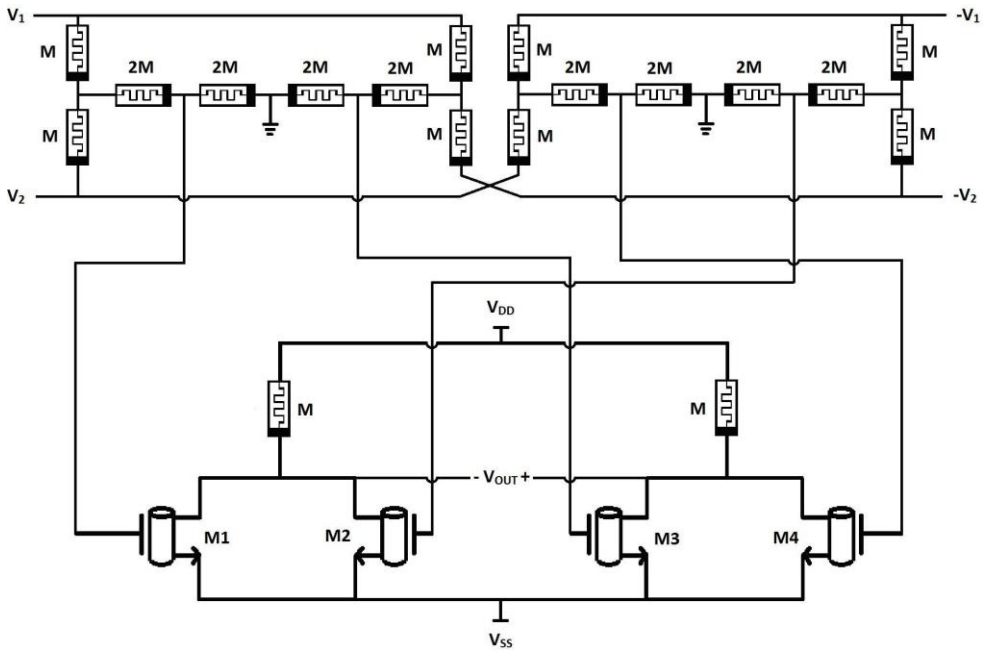

Figure 7.2: Proposed Multiplier circuit.

7.4 Simulation Results

The proposed memristor and CNFET based multiplier circuit is designed and simulated using HSPICE simulator incorporating 32nm CNFET model [171] and memristor model [172] at a supply voltage of ±0.3V . The performance of the multiplier such as power, linearity and bandwidth are severely affected by the diameter of the CNTs. The diameter of CNT (D_{CNT}), its bandgap energy Eg and the threshold voltage of the device (V_{th}) are related by the following equations

$$Eg = 0.84\ eV / D_{CNT} \tag{7.7}$$

$$V_{th} = Eg / 2e \tag{7.8}$$

Where 'e' is the electronic charge. D_{CNT} not only affects the source/drain series resistance but also the threshold voltage of CNFET. It is observed from the simulation results that with the increase in the diameter of the nanotube as shown in Figure 7.3, bandwidth, and power consumption of the multiplier increase. These trends can be justified by the decrease in the gate to channel capacitance along with fringe capacitance. This decrease in capacitance is due to enhanced screening between adjacent CNTs [49, 134]. However, it is to be noted that for large values of D_{CNT}, the

current saturates because of large screening and scattering effects thereby severely affecting the linearity of the circuit. The CNTs are therefore optimized for their most practical values, a compromise between circuit requirements and a trade-off is involved between the 3-dB bandwidth, power and linearity. The optimum diameter value is hence chosen to be 0.9 nm corresponding to chiral vector (11, 0). Table 7.1 and 7.2 show the optimized CNFET and memristor parameters used in the simulation of the proposed multiplier. The performance evaluation of the multiplier is carried out on the basis of key parameters namely DC transfer characteristics, harmonic distortion analysis, frequency response, low voltage operation, low power consumption and noise analysis at a supply voltage of ±0.3V corresponding to a input of 0.1V.

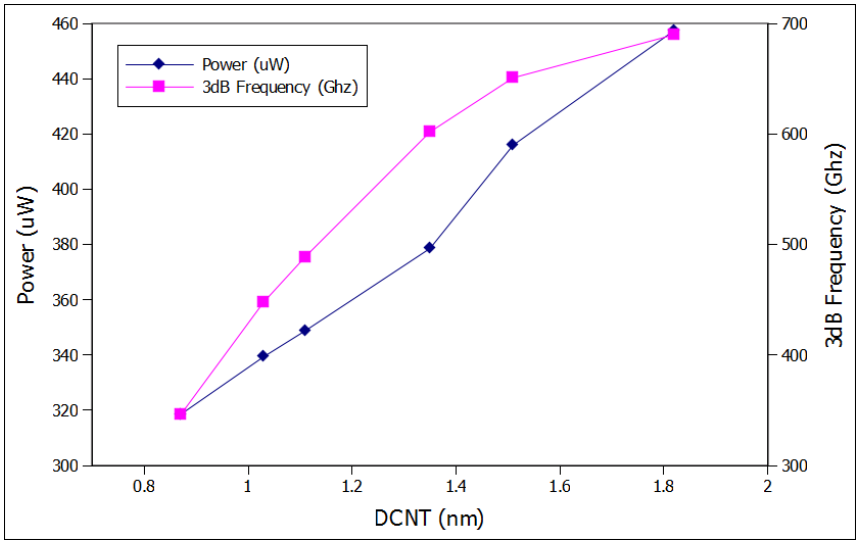

Figure 7.3: CNT diameter versus 3-dB Bandwidth/Power.

Table 7.1: Device Parameters of a CNFET

CNFET parameter	Value
Physical channel length (L_{ch})	32nm
Length of doped CNT source/drain extensions	32nm
Diameter of CNT	0.9nm
Gate dielectric	HfO_2
Dielectric constant	16
Chirality of tube	(11, 0)
T_{OX}	4nm
Pitch	20nm

Table 7.2: Device Parameters of a Memristor

Memristor parameter	Value
ON resistance	1k
OFF resistance	10k
p (positive integer)	1
Average Dopant Mobility μ_v	$10^{-14}\ m^2 s^{-1} V^{-1}$
Total width of memristor '*D*'	10nm

7.4.1 Low Voltage Operation and Reduced Power Consumption

The proposed multiplier circuit is operated at input supply voltage of ±0.3V. This shows that the circuit is capable of low voltage operation and hence low power consumption of the circuit can be achieved. This low voltage operation of the proposed circuit is due to the use of single stacked transistor along with a memristor connected load unlike the other low voltage mode multipliers that use double stacked transistors [173-176]. Thus, it can be operated at a voltage as low as ±0.3V with moderate linearity. Figure 7.4 and Figure 7.5 show the power consumption of the proposed circuit for input supply voltage and input voltage respectively. The power consumption of the circuit can be as low as 43.8 μW corresponding to the inputs of 0.1V (V1 and V2) at ±0.3V power supply. These features of the proposed circuit make it suitable for battery operated portable devices especially for biomedical applications.

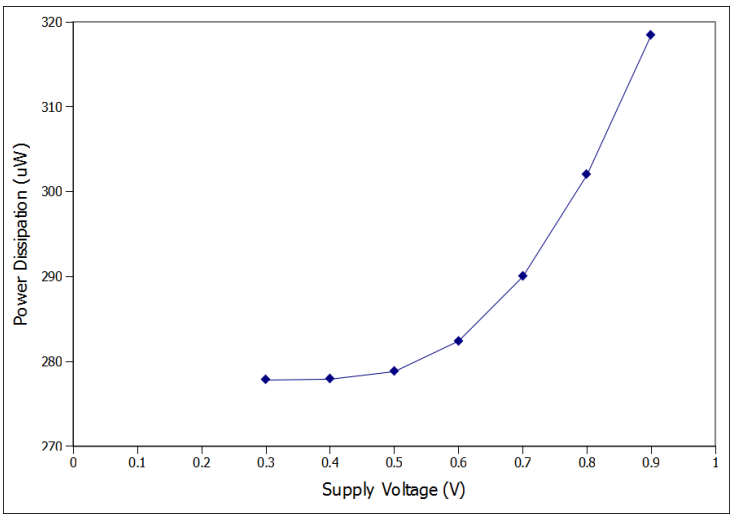

Figure 7.4: Power dissipation with supply voltage.

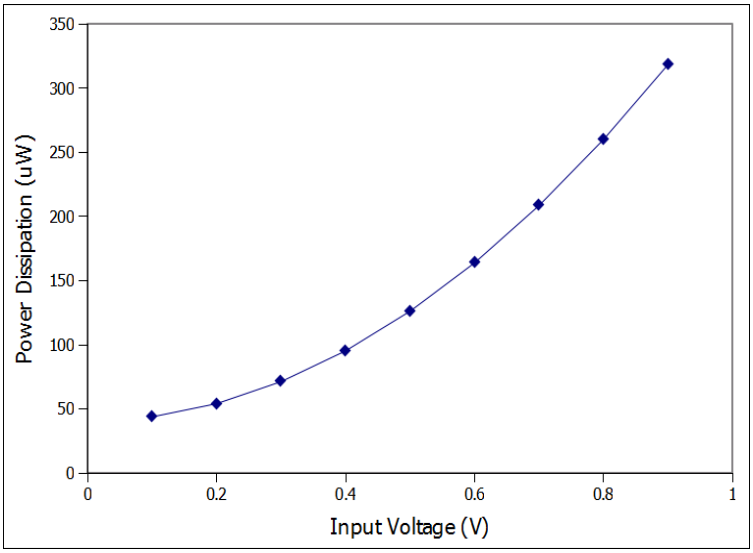

Figure 7.5: Power dissipation with input voltage.

7.4.2 DC Transfer Characteristics

Figure 7.6 shows simulated DC transfer characteristics of the proposed multiplier, when V1 was swept continuously from -0.3V to 0.3V while V2 was varied from -0.3V to 0.3V with 60mV step size. It can be observed that the linear range of the circuit is approximately ±0.25V.

7.4.3 Frequency Response

To measure the frequency characteristics of multiplier, the proposed circuit is operated in frequency doubler configuration. A Sine wave of 0.1V peak value is given as inputs to both V1 and V2. Figure 7.7 shows the typical frequency response curve. It is observed that the high-3DB frequency of 30.5 GHz is obtained from the simulated curve. This high bandwidth is attributed to the use of memristors as voltage divider elements and also to the low intrinsic capacitance of the CNFET as compared to the bulk CMOS [177].

7.4.4 Harmonic Distortion Analysis

Figure 7.8 depicts the transient response of the multiplier in frequency doubler configuration. In this configuration, a 0.1V amplitude sinusoidal signal of 1MHz frequency is given as input to both V1 and V2. The harmonic distortion analysis is then performed. Figure 7.9 shows the variation of THD as a percentage of the output

for different values of input. The simulated maximum THD is about 0.75% with a input range of ±0.25V.

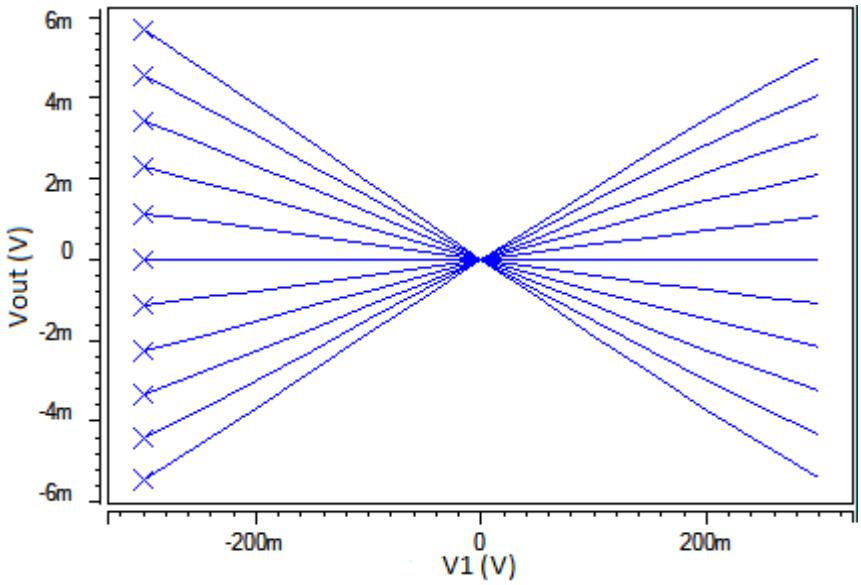

Figure 7.6: DC Transfer Characteristics.

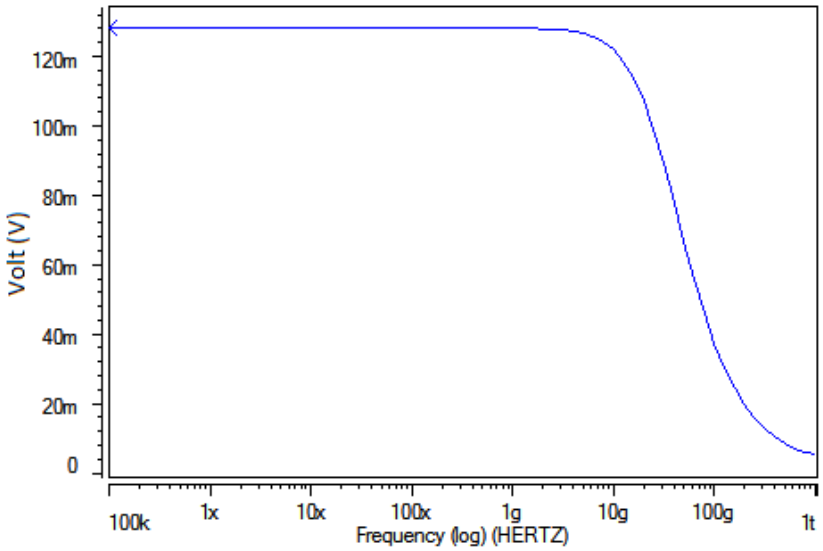

Figure 7.7: Frequency Response of Multiplier.

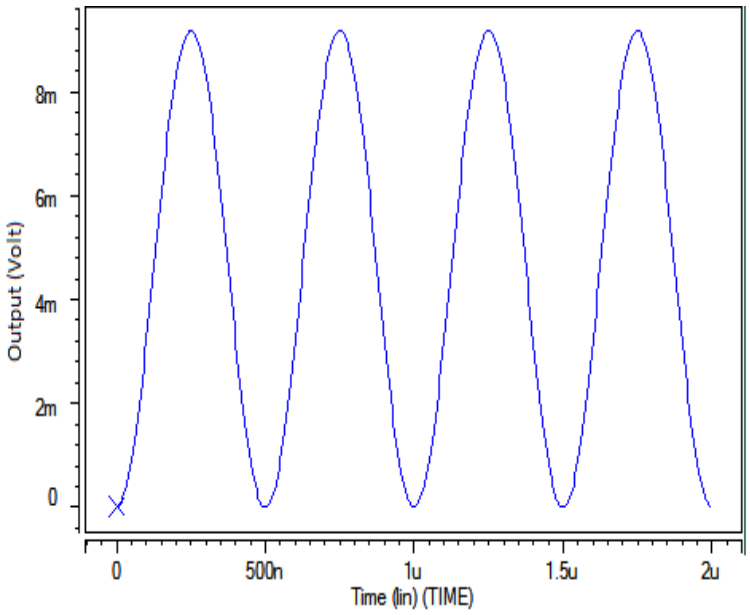

Figure 7.8:Transient Response of a Multiplier.

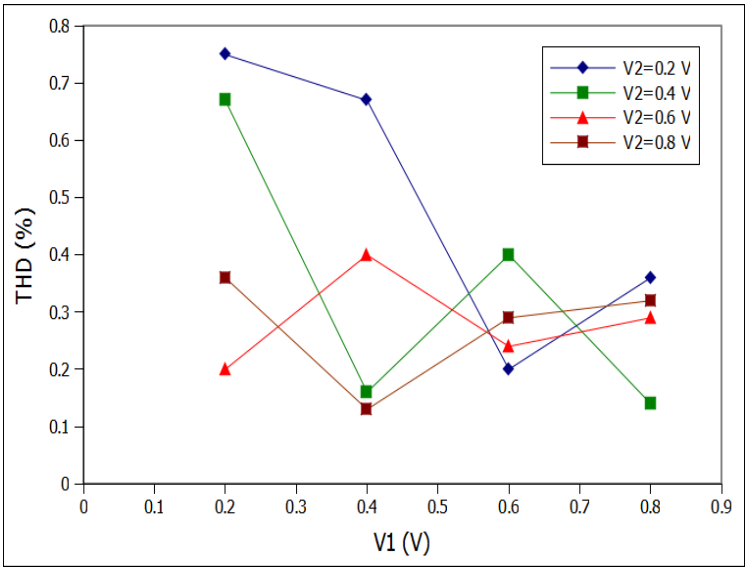

Figure 7.9: THD output Variation with inputs of Multiplier.

7.4.5 Noise Analysis

The equivalent input and output noise simulation is performed with the input sine wave of 0.1V in the frequency doubler configuration of the proposed multiplier. The results are plotted in Figure 7.10 and Figure 7.11 respectively. The results are in good agreement showing significant suppression of noise. The proposed multiplier uses minimal number of devices and this result in significant noise suppression.

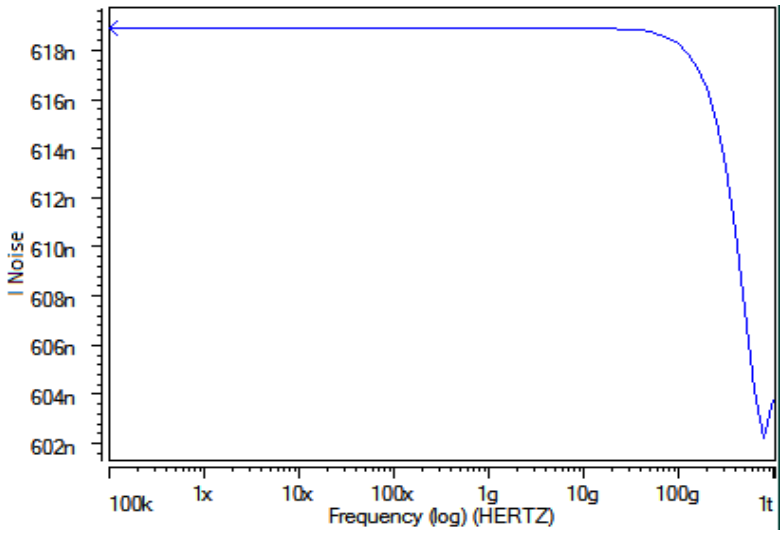

Figure 7.10: Equivalent input noise in (V/√Hz).

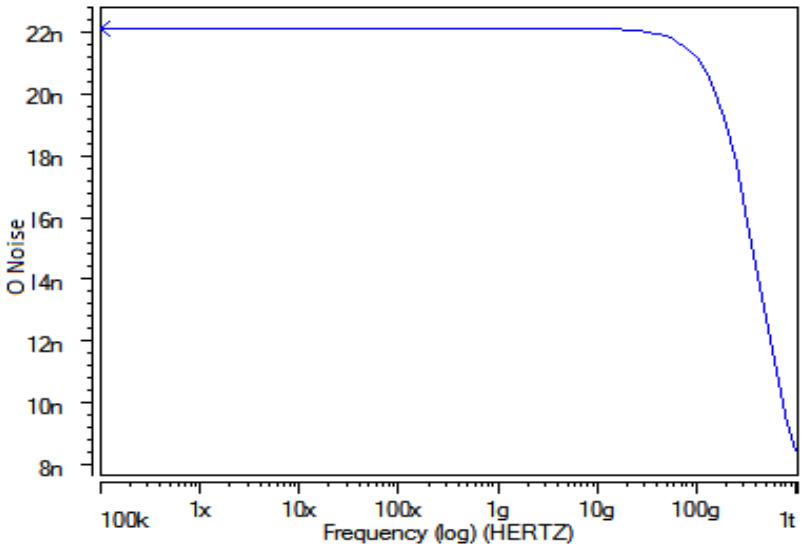

Figure 7.11: Equivalent output noise in (V/√Hz).

7.4.6 Proposed Multiplier as Amplitude Modulator

An important application of the proposed multiplier is the use of the circuit as amplitude modulator. Sinusoidal inputs of 0.1V are applied at the two inputs V1 at 1MHz and V2 at 10MHz respectively. Figure 7.12 shows the modulation performance.

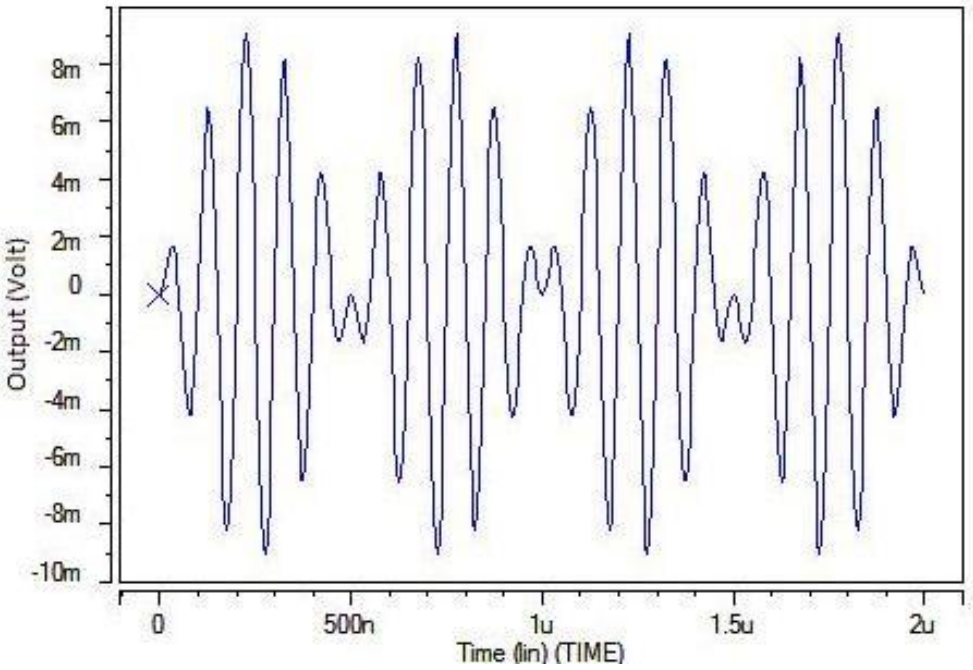

Figure 7.12: Amplitude Modulation Waveform for 0.1V 1MHz input and 10MHz carrier.

7.4.7 Comparison with Previous Implementations

Table 7.3 summarizes the comparison of the proposed multiplier with other previous work on CMOS and CNFET based multipliers. The 32nm CMOS multiplier performance parameters are also listed for better comparison. The proposed multiplier is found to be better in most of its performance measures as compared to the others. Depending upon applications, there is a trade-off between certain parameters.

Table 7.3:Comparison of the Previous Work with the Proposed Work

Parameters	**Proposed Work**	**Makwana *et.al***	**Sawigun *et. al* 32 nm Design**	**Sawigun *et. al***	**Kiatwarin *et.al***	**Hidayat *et.al***
Technology node	**CNFET 32nm**	**CNFET 32nm**	**CMOS 32nm**	**CMOS 0.35µm**	**CMOS 0.35µm**	**CMOS 0.18µm**
Voltage supply	±0.3V	±0.9V	±0.9V	+1.8V	+1.5V	±1V
Transistor count	4	6	10	10	10	36
Input range	±0.25V	±0.4V	±0.25V	±0.4V	±0.4V	±0.1V
3dB bandwidth	30.5 GHz	49.88 GHz	0.7GHz	10MHz	95MHz	3.96GHz
THD% at 1MHz	≤0.75	≤ 0.45	≤0.8 at 25KHz	≤1.0 at 25KHz	≤1.0	≤1.0
Power consumption	43.8 µW at 0.1V inputs	246.9 µW	50 µW	200µW	46.4 µW	588 µW

7.5 Summary

This chapter presents a reconfigurable differential four quadrant analog multiplier based on memristors and carbon nanotubes FETs which is capable of high bandwidth and low power operation. We are not claiming that our proposed circuit is better in all respect than the others in the literature. Rather we are determining how well our circuit can be used for low power applications without sacrificing its bandwidth and linearity. Extensive simulations using optimized CNFET and memristor models have proved the superior performance of most of the parameters of this multiplier in comparison to the other CMOS and CNFET based multipliers, making it viable for low power applications.

The next chapter summarizes the conclusions drawn from this thesis. It also highlights the major achievements of this work and areas of future work in the field of devices beyond bulk CMOS.

CHAPTER 8

Summary and Conclusions

Chapter 8

SUMMARY AND CONCLUSIONS

After more than 40 years of aggressive downsizing of MOSFETs, geometric scaling is reaching fundamental limits. Presently, it is facing even more obstacles, which are more severe than the earlier ones. Various short channel effects and static power dissipation are few of them. Also, with the advent of body based sensor networks, RFIDs, implantable medical electronics etc., ultra low power portable market is expanding at a rapid pace. Therefore, there is a need to explore CMOS operating in subthreshold regime and also exploring non-CMOS devices to meet the power and throughput targets. Subthreshold region of operation is ideal for ULP applications because a subthreshold circuit shows an order of magnitude power saving over superthreshold circuits. Hence, the aim of this thesis is to enhance the speed and robustness of subthreshold circuits by optimizing CMOS devices and also to look for future devices that could replace the existing bulk CMOS technology in near future.

8.1 Introduction

This chapter is organized into four sections. The first section presents the summary of the work presented in each chapter. The second section provides the conclusions drawn from the results obtained in each chapter. The third section summarizes the achievement and the last section outlines areas for future research.

8.2 Summary

For Ultra low power applications, extremely low power allowance and moderate throughput are the key requirements. Power dissipation, therefore has transpired as a critical design challenge. The most effective way to reduce the power consumption is to operate the transistor in subthreshold region. Nevertheless, subthreshold circuits are extremely slow and are more prone to PVT variations. Moreover, in order to continue CMOS scaling, new innovations and device design will be required other than the bulk CMOS. Hence, this thesis mainly targets TFET and CNFET devices and their performance evaluation at lower supply voltages thereby, leading to lower OFF state leakage and power dissipation than CMOS at the same supply voltage. It also explores

the design of subthreshold CCII so that the current mode feature of the CCII can be utilized in ULP applications. The summary of this thesis is highlighted in this section.

Chapter 2 presented a brief overview of technology scaling and sources of power dissipation. For the CMOS technology to continue its dominance in semiconductor industry, the industry must adopt new techniques to reduce leakage power dissipation. At the device level, TFET and CNFET were chosen as emerging devices that could possibly replace the existing CMOS technology. A brief introduction of TFET and CNFET were presented followed by selected reviewed prior research work.

Almost all Application Specific Integrated Circuit (ASIC) libraries are designed and optimized for superthreshold circuits at a technology defined V_{DD}. This nominal V_{DD} limits the aggressive scaling of V_{th} and T_{OX} for superthreshold circuits to minimize the subthreshold and gate leakage current. However, gate leakage current is less critical under subthreshold conditions due to lower V_{DD}. Such high V_{th} and T_{OX} of the device reduces the subthreshold drive current and I_{ON}/I_{OFF} when operated in subthreshold region. These devices may not give the best performance for subthreshold circuits. Hence, the optimization of Si-MOSFET device is presented for subthreshold circuits at 45 nm technology node using Synopsys TCAD tools in Chapter 3. This optimized device gives best performance under subthreshold conditions.

There is a need of a basic building block that can be used to implement large number of different analog functions and that too in the subthreshold region. Second generation current conveyor (CCII) can be regarded as a real competitor for the operational amplifier (OPAMP). Though, significant amount of work was published to improve the performance of CCII for superthreshold circuits, CCII performance investigation and optimization under subthreshold condition has been largely ignored by the research community. Hence, chapter 4 of this thesis explored the design of CCII under subthreshold condition at 32 nm CMOS technology.

In this era of nanotechnology, it is expected that emerging devices like TFET and CNFET will replace the existing bulk CMOS technology in the future. Operating the Si-MOSFET in subthreshold region degrades the circuit performance in terms of speed and robustness against PVT variations. This may cause the subthreshold circuit failure at very low V_{DD}. Hence, this thesis also investigated the suitability of most emerging devices like TFET and CNFET for their performance evaluation for

subthreshold circuits. In Chapter 5, it is demonstrated that TFET based CCII and INA outperformed their CMOS based counterparts at low voltage subthreshold operation in terms of gain and bandwidth. Chapter 6 proposed CNFET based 6T SRAM cell in 22nm technology node to evaluate CNFET based design. The investigation revealed that CNFET based single-ended 6T SRAM cell saves dynamic as well as static power and maintains higher read stability at the cost of acceptable read/write delay. It proves its robustness by exhibiting narrower spread in various design metrics than CMOS based design. This is due to the cylindrical geometry of CNFET.

Chapter 7 presented the design of four quadrant voltage multiplier based on another emerging device memristor together with CNFET. The proposed design offered large input range, extremely high bandwidth and very small power consumption at 32nm technology node.

8.3 Conclusions

This thesis explored CMOS, TFET, CNFET and memristor devices and the circuits based on those devices under subthreshold conditions. The work presented in this thesis will enable to operate real time portable applications having moderate speed and low power requirement under subthreshold conditions. It has also explored the designs of subthreshold CCII, SRAM and Multiplier so that their features can be extended to the ULP domain. This section highlighted different conclusions drawn from the research work carried out in this thesis.

The CMOS scaling, sources of power consumption and subthreshold operating region are well-studied in Chapter 2. It is concluded that in order to continue CMOS scaling and reduced power dissipation in CMOS, it is necessary to explore emerging devices like TFET and CNFET to extend the density and performance of integrated circuits.

The existing CMOS devices are fully optimized for superthreshold region of operation. It is therefore, very important to look into their performance evaluation under subthreshold conditions. To cope up with the above challenge, Chapter 3 proposed bulk NMOS and PMOS devices optimized using Synopsys TCAD tool especially for subthreshold operating region which shows 9.89% and 34% improvement in subthreshold slope and I_{ON}/I_{OFF} ratio respectively over their corresponding superthreshold device at the same technology node.

Chapter 4 explored the performance of subthreshold CCII using both the minimal and non-minimal lengths of transistors and various performance parameters have been evaluated keeping all the transistors in the subthreshold regime. It also demonstrated that design 4 with $L=6L_{min}$, operating at ±0.25V and at a bias current of 20pA, was found to be optimal and more robust as compared to other designs. Furthermore, variability analysis, which is crucial under subthreshold condition, has also been carried out.

Chapter 5 reported a comparative study of CMOS and TFET based Second Generation Current conveyor (CCII) at a supply voltage of ±0.3V and bias current of 1nA at 32nm technology node. The TFETs (both n and p type) are designed with the channel length of 25nm and 1nm of high-K dielectric. The performance comparison of TFET and CMOS based CCII shows that TFET based design outperformed their CMOS based counterparts at low voltage subthreshold operation in terms of gain and bandwidth.

Chapter 6 proposed CNFET based single ended 6T SRAM cell which is capable of saving dynamic and static power at 22nm technology node. The use of appropriate D_{CNT} (diameter of CNFET) and hence V_t is a critical piece of our design strategy. It consumes 2.25 × lower standby power. It proves its robustness against process variations by featuring 2.15× narrower spread in standby power distribution. Our bitcell showed 2.38× improvement in RSNM. The proposed design incurs 1.25× longer read delay and 1.15× longer write delay compared to 6T, but at the same time it showed its robustness by offering 1.67× narrower spread in read delay and 1.12× narrower spread in write delay respectively.

Chapter 7 proposed a reconfigurable four quadrant multiplier based on memristor and CNFET. It can be concluded from the results that the proposed multiplier has an input range of ±0.25V, extremely large bandwidth of 30.5 GHz, and consumes just 43.8μW of power along with low total harmonic distortion (THD% ≤0.75) and significant noise suppression at a supply voltage of ±0.3V.

8.4 Achievements

This section lists out some of the major achievements of this piece of research work.

- Majority of nanoscale devices are optimized for superthreshold operation and they fail to deliver their best performance under subthreshold conditions. Hence, this thesis proposed an optimized NMOS and PMOS device for subthreshold conditions with much better subthreshold leakage current and subthreshold slope to enhance the speed of subthreshold circuits using Synopsys TCAD tool.

- It then explored a new subthrehold design style of CCII. To the best of our knowledge CCII design, performance and characteristics have not yet been explored under subthreshold condition. Hence, this thesis investigates, for the first time, the design and optimization of a CCII under subthreshold condition.

- The design and optimization of a tunnel FET based CCII is carried out for the first time in this thesis and the results are compared with its CMOS counterpart.

- An optimized CNFET based 6T SRAM cell in 22 nm technology is proposed. The optimized CNFET design outperforms its CMOS counterpart in terms of most of its design metrics.

- It has also proposed a reconfigurable memristor and optimized CNFET based low voltage, low power four quadrant analog multiplier. The proposed design proved the superior performance of most of the parameters of this multiplier in comparison to the other CMOS and CNFET based multipliers making it suitable for low power applications.

8.5 Future work

Although, this work reports promising emerging device level solution for reducing power dissipation and extending CMOS scaling, there is still a large scope of future work that can be taken up in this area.

- The biggest future challenge is to successfully design and fabricate fully-optimized Tunnel FETs of both n-type and p-type , that show low off-currents beyond what is possible for conventional MOSFETs, high ON-currents, and average subthreshold swings of less than 60 mV/decade at room temperature. If Tunnel FETs are to be used as a conventional MOSFET replacement, the on

current must be boosted to ITRS roadmap levels by some technique that reduces the band gap at the tunnel junction. Further work will also be necessary in order to develop accurate analytical and compact models for Tunnel FETs. Although some work has been done in these areas.

- Spintronics or spin transistors are the new concept device that utilize spin instead of charges to store the information. The interesting feature of spin transistors are nonvolatile storage of information and reconfigurable output characteristics which make them suitable for various functionalities in the neuromorphic domain. These features raise hope of building analog neuromorphic circuits by exploiting the unique characteristics of spin devices.

- Nanowire and multi-gate devices are promising devices for future technology nodes that can provide electrostatic integrity for controlling the short channel effects. Nanowire field effect transistor (NWFET) is a FET in which the conventional planar MOSFET channel is replaced with a semiconducting nanowire. One extension of this work may be designing NWFET in TCAD and various analog building blocks in subthreshold regime may be realized using it to reduce leakage power.

- 2D material like graphene, MoS_2 are promising candidates for low power, high speed devices, and can offer some advantage over Si devices in gate delay, *ft* and power dissipation. It is important to explore the design of circuits under subthreshold conditions using these futuristic devices.

- Design techniques usually employed for VLSI circuits are worthless unless integrated in design automation flow. Since subthreshold logic appears to be the most promising one for ULP consumer electronics market, therefore the first step to validate extensive adoption of subthreshold design is to characterize standard-cell libraries by the vendors at V_{DD} below V_{th}. Design guidelines are needed to be explored in order to select the optimum values of V_{DD}, $V_{th,}$ $T_{OX,}$ L_g, substrate, source/drain, and halo doping so as to achieve best performance of subthreshold devices at different technology nodes.

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